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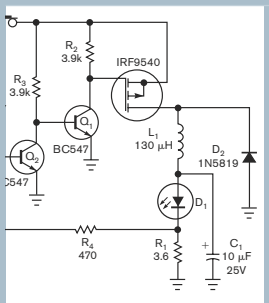

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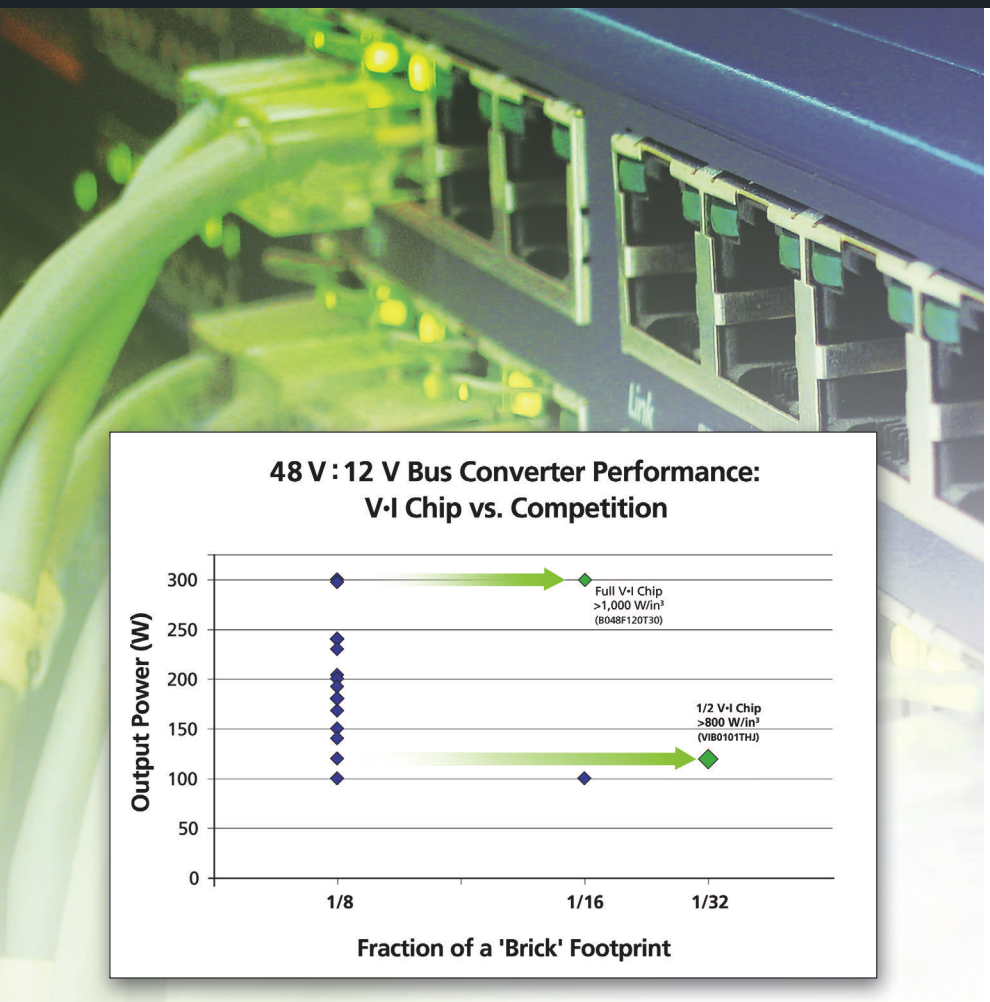

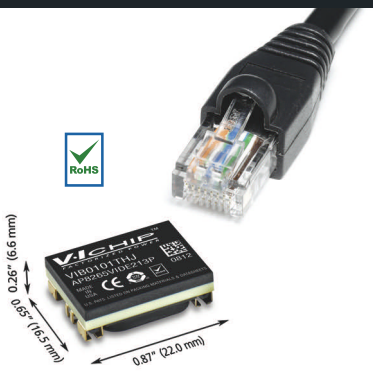

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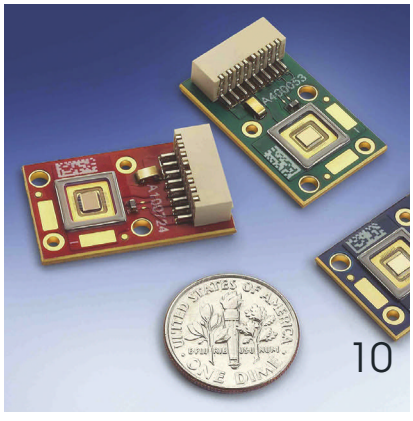

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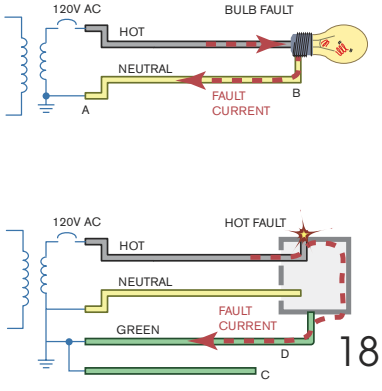

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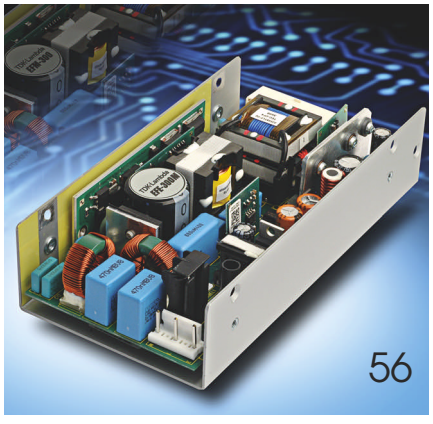

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EDN® (ISSN#0012-7515), (GST#123397457) is published biweekly, 24 times per year, by Reed Business Information, 8878 Barrons Blvd, Highlands Ranch, CO 80129-2345. Reed Business Information, a division of Reed Elsevier Inc, is located at 360 Park Avenue South, New York, NY 10010. Tad Smith, Chief Executive Officer; Mark Finkelstein, President, Boston Division. Periodicals postage paid at Littleton, CO 80126 and additional mailing offices. Circulation records are maintained at Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Telephone (303) 470-4445. POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80163-7500.

Rates for nonqualified subscriptions, including all issues: US, $179.99 one year; Canada, $229.99 one year (includes 7% GST, GST#123397457); Mexico, $229.99 one year; air expedited, $399.99 one year. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. Publications Agreement No. 40685520. Return undeliverable Canadian addresses to: RCS International, Box 697 STN A, Windsor Ontario N9A 6N4. E-mail: Subsmail@ReedBusiness.com. Please address all subscription mail to EDN®, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345.

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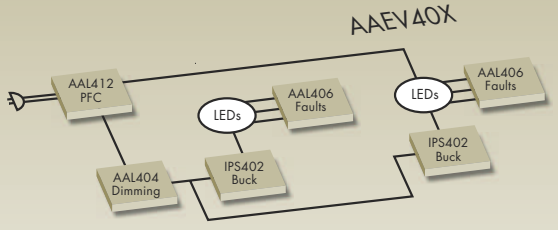

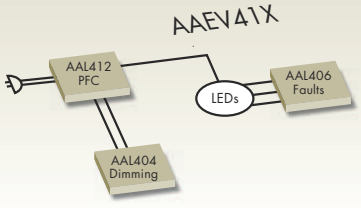

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Tech salaries increasing, despite economy
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→www.edn.com/article/CA6637653

Wind power, telecom-energy usage, plus solar hitting bottom
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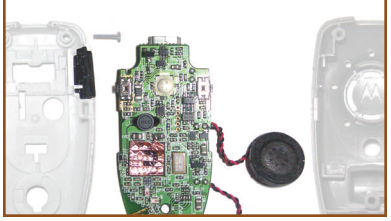
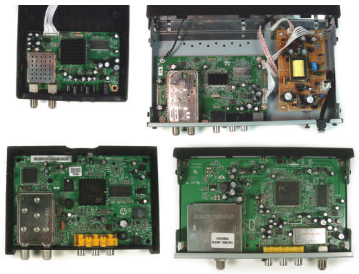




READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

The ATSC coupon-eligible converter box: a consumer-electronics case study
The pending NTSC shutoff has US consumers clamoring for rebate-eligible hardware that will stave off the loss of over-the-air television. How do manufacturers distinguish themselves from opponents in such a hypercompetitive market?
→www.edn.com/article/CA6632369

DisplayPort versus HDMI: Do we really need two digital-display-interface standards?
→www.edn.com/article/CA6594089

Intel invests $7 billion in US manufacturing, supports 7000 jobs as it looks to 32 nm
→www.edn.com/article/CA6636226

Top 10 OEMs consume a third of all semiconductors, Gartner reports
→www.edn.com/article/CA6635915

DSP-directory gold mine
Technical Editor Robert Cravotta's annual directory of DSP devices and cores is impressive in print (pg 28), but take a look at the megasized online version. It includes **tables** that allow you to do side-by-side product comparisons and select just the right device for your project. Dig in; who knows what hidden treasure you'll uncover?
→www.edn.com/dspdirectory

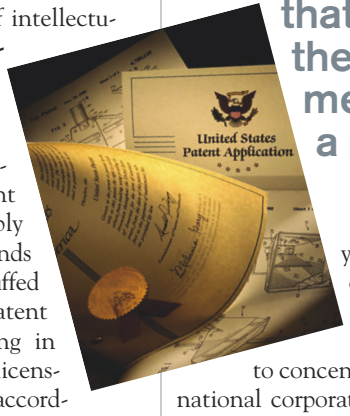
BY PAUL RAKO, TECHNICAL EDITOR

Time for a change in patent law

The inventions of Scottish inventor and engineer James Watt in the late 18th and early 19th centuries led to the improvement of the steam engine and, ultimately, to the Industrial Revolution. So, it was with sadness that I read recently that he played the patent system like a violin to make himself rich with licensing fees while suppressing important improvements. This behavior continued until the time limits on the patents ran out, at which time a huge surge of innovation pushed England into the industrial age and provided plenty of tax money in the process. Economists Michele Boldrin and David K Levine make these observations in their free online book about the difficulties of intellectual-property law (**Reference 1**). In a more recent example, the late inventor Jerome Lemelson emulated Watt's behavior: "He didn't invent anything new; he simply looked for technical trends and submitted overstuffed claims that baffled patent examiners" while raking in nearly $1.5 billion in licensing fees and royalties, according to a 2001 article (**Reference 2**).

I don't think that everything should be free. But a 20-year government-enforced time limit on patents imposes a long monopoly for the patent holder and does not promote the arts and sciences, as the Constitution of the United States says it should: "To promote the Progress of Science and useful Arts, by securing for limited Times to Authors and Inventors the exclusive Right to their respective Writings and Discoveries" (**Reference 3**).

One of the biggest problems with the patent system is that it forces the government to pick a winner.



Contrary to what you might think, patent laws are not in place to help the little guy; they exist to concentrate power in multinational corporations. I'm not saying that you shouldn't be able to get a patent. I'm just saying that, if the Constitution authorizes patents to promote the arts, then the term should be closer to one year than to 20 years. This fact should be obvious to anyone who has kept track of modern technology. The Betamax-versus-VHS videotape battle happened because each company had patents that it wanted to incorporate into the next world standard. We have seen a rehash of this scenario in the Blu-ray-versus-HD-DVD (high-definition-digital-video-recorder) battle, which companies are fighting not to benefit consumers but to reap the monopoly of profits from the suite of patents in the systems. In another example, we are soon going to be converting to a needlessly complex and outmoded digital-TV standard that is subject to interference because those who conspired to shove it down our throats were interested not in giving us the best technology but instead in tying up the scheme with their patents so that they can make licensing revenue for 20 years.

One of the biggest problems with the patent system is that it forces the government to pick a winner, and the winner takes all. It is proper to credit a Texas Instruments employee, the late Jack Kilby, with important contributions to the integrated circuit. But the late silicon-transistor pioneer and Fairchild co-founder, Jean Hoerni, and the late Bob Noyce, co-founder of both Fairchild and Intel, made contributions just as essential as Kilby's to the modern IC.

The US patent system was broken from the start, if only because we emulated the British system, as the Watt story so superbly demonstrates. If we want to boost the economy and make a lot of jobs for engineers, the best thing we could do is severely limit the terms of patents and make them more difficult to obtain. EDN

REFERENCES

1. Boldrin, Michele, and David K Levine, *Against Intellectual Monopoly*, www.dklevine.com/general/intellectual/againstfinal.htm.
2. Titus, Jon, "Invalidate Lemelson's patents," *Test & Measurement World*, July 2001, www.tmworld.com/article/CA189010.
3. Morris, Gouverneur, James Madison, et al, *Constitution of the United States of America*, Article 1, Section 8, Clause 8.

Contact me at paul.rako@edn.com.

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PRESIDENT, BOSTON DIVISION, REED BUSINESS INFORMATION
Mark Finkelstein, mark.finkelstein@reedbusiness.com
1-781-734-8431

PUBLISHER, *EDN* WORLDWIDE
Russell E Pratt, 1-781-734-8417;
rpratt@reedbusiness.com

ASSOCIATE PUBLISHER, *EDN* WORLDWIDE
Judy Hayes, 1-408-421-3799;
judy.hayes@reedbusiness.com

VICE PRESIDENT, EDITORIAL DIRECTOR
Karen Field, 1-781-734-8188;
kfield@reedbusiness.com

EDITOR-IN-CHIEF, *EDN* WORLDWIDE
Rick Nelson, 1-781-734-8418;
rnelson@reedbusiness.com

EXECUTIVE EDITOR
Ron Wilson, 1-408-345-4427;
ronald.wilson@reedbusiness.com

MANAGING EDITOR
Amy Norcross
1-781-734-8436; fax: 1-720-356-9161;
amy.norcross@reedbusiness.com
Contact for contributed technical articles

SENIOR ART DIRECTOR
Mike O'Leary
1-781-734-8307; fax: 1-303-265-3021;
moleary@reedbusiness.com

ANALOG
Paul Rako, Technical Editor
1-408-745-1994; paul.rako@edn.com

EMBEDDED SYSTEMS
Warren Webb, Technical Editor
1-858-513-3713; fax: 1-858-486-3646;
wwebb@edn.com

MASS STORAGE, MULTIMEDIA, PCs, AND PERIPHERALS
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MICROPROCESSORS, DSPs, AND TOOLS
Robert Cravotta, Technical Editor
1-661-296-5096; fax: 1-303-265-3116;
rcravotta@edn.com

NEWS
Suzanne Deffree, Managing Editor
1-631-266-3433;
sdeffree@reedbusiness.com

POWER SOURCES, ONLINE INITIATIVES
Margery Conner, Technical Editor
1-805-461-8242; fax: 1-805-461-9640;
mconner@reedbusiness.com

DESIGN IDEAS EDITOR
Martin Rowe,
Senior Technical Editor,
Test and Measurement World
edndesignideas@reedbusiness.com

SENIOR ASSOCIATE EDITOR
Frances T Granville
1-781-734-8439; fax: 1-303-265-3131;
f.granville@reedbusiness.com

ASSOCIATE EDITOR
Maura Hadro Butler, 1-617-276-6523;
mbutler@reedbusiness.com

EDITORIAL/WEB PRODUCTION
Diane Malone, Manager
1-781-734-8445; fax: 1-303-265-3024
Steve Mahoney, Production/Editorial Coordinator
1-781-734-8442; fax: 1-303-265-3198
Melissa Annand, Newsletter/Editorial Coordinator
1-781-734-8443; fax: 1-303-265-3279
Adam Odoardi, Prepress Manager
1-781-734-8325; fax: 1-303-265-3042

CONSULTING EDITOR
Jim Williams, Staff Scientist,
Linear Technology

CONTRIBUTING TECHNICAL EDITORS
Dan Strassberg, strassbergedn@att.net
Nicholas Cravotta, editor@nicholascravotta.com

COLUMNISTS
Howard Johnson, PhD, Signal Consulting
Bonnie Baker, Texas Instruments
Pallab Chatterjee, SiliconMap

PRODUCTION
Dorothy Buchholz, Group Production Director
1-781-734-8329
Joshua S Levin-Epstein, Production Manager
1-781-734-8333; fax: 1-781-734-8096

EDN EUROPE
Graham Prophet, Editor, Reed Publishing
The Quadrant, Sutton, Surrey SM2 5AS
+44 118 935 1650; fax: +44 118 935 1670;
gprophet@reedbusiness.com

EDN ASIA
Susie Newham, Managing Director
susie.newham@rbi-asia.com
Kirtimaya Varma, Editor-in-Chief
kirti.varma@rbi-asia.com

EDN CHINA
William Zhang, Publisher and Editorial Director
wmzhang@idg-rbi.com.cn
John Mu, Executive Editor
johnmu@rbichina.com.cn

EDN JAPAN
Katsuya Watanabe, Publisher
k.watanabe@reedbusiness.jp
Ken Amemoto, Editor-in-Chief
amemoto@reedbusiness.jp

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Reed Electronics Group

pulse

INNOVATIONS & INNOVATORS

LED chip sets help pico projectors bring big displays to small devices

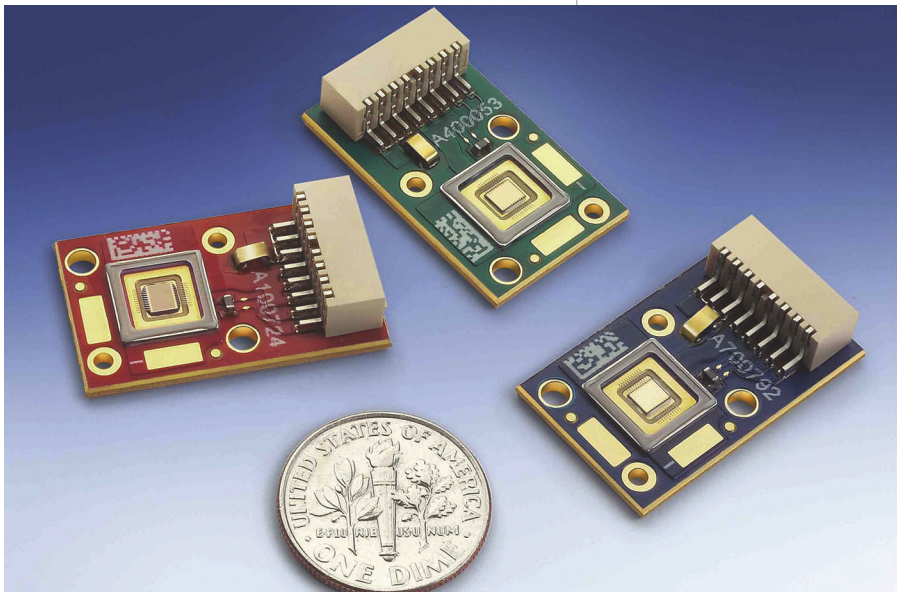
Pico projectors, LED-based devices small enough to fit into an MP3 player or even a slightly oversized cell phone, were prominently on display at the CES (Consumer Electronics Show) in Las Vegas both this year and last. The obvious use for this type of projector is to show impromptu screenings of your YouTube videos or in-your-face slide shows to a group of friends—in the same way that you currently use full-sized projectors. Unlike the large projectors, however, pico devices can make any surface a sign, an art installation, or a call to action and thus may usher in entirely new applications.

An example of a dedicated pico projector is the GP1 from BenQ. The GP1 uses the Luminus PhlatLight LED PT-39 chip set, which includes one red, one green, and one blue LED on each chip of the three-chip set. The chip set works with handheld-projection devices with microsized displays ranging from 0.4 to 0.55 in. wide. The GP1, for example, provides 100 lumens of light to project a 10- to 80-in.-wide image onto a nearby wall or screen and boasts a 20,000-hour "lamp" life. The BenQ GP1 pico projector will be available in March for $499.

With its DLP (digital-light-processing) chips, TI is also addressing the pico-projector market. The MEMS (microelectromechanical)-based light-switching engines power the company's current generation of projectors. The company recently announced a pico-projector development kit that includes a DLP pico-projection engine, a power supply, the necessary video cables, and a three-LED light source. The kit interfaces with the Beagle Board, which employs a TI OMAP (open-multimedia-application-processor) 35x running Linux. The kit sells for $349; the Beagle Board sells for $149.

—by Margery Conner

- **BenQ**, www.benq.com.
- **Luminus**, www.luminus.com.
- **Texas Instruments**, www.ti.com.



The PhlatLight LED PT-39 chip set from Luminus replaces arc lamps in projector systems, including pocket-sized pico projectors.

FEEDBACK LOOP

"Over the last six months, I've bought five brands of converters, and only one ... is still working. I got so frustrated (that) I tossed anything that had to do with analog and purchased TVs and recorders that had built-in digital tuners."

—EMS manufacturing manager and *EDN* reader Scott McKee, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6632369. Add your comments.

Scope-based audio-bus, power-analysis tools target embedded-system designers

Tektronix has announced a triggering-and-analysis module for serial-digital-audio buses and a new power-analysis module. The modules plug into the company's DPO (digital-phosphor-oscilloscope) 3000 and MSO (mixed-signal-oscilloscope)/DPO4000 Series and enable the use of analysis capabilities that reside in the firmware of the instruments, which offer bandwidths as high as 1 GHz. The capabilities automate measurement-and-analysis tasks on digital-audio buses and switch-mode power supplies, simplifying and speeding troubleshooting and debugging of new designs.

Switch-mode power supplies require several specialized tests that take both time and expertise. The DPOxPwr module incorporates automated features that quickly perform these tests without complicated programming. Similarly, the DPOxAudio module addresses the needs of designers who integrate digital-audio capabilities into products such as toys, gaming systems, mobile phones, and professional-recording consoles. These designs use I²S (inter-IC-sound) and TDM (time-division-multiplexed) serial-bus protocols. For efficient debugging, the DPOxAudio module instantly decodes the protocol, time-aligns the waveform and decoded-packet data on the scope display, and then automatically triggers on and searches for packet-level content that you specify.

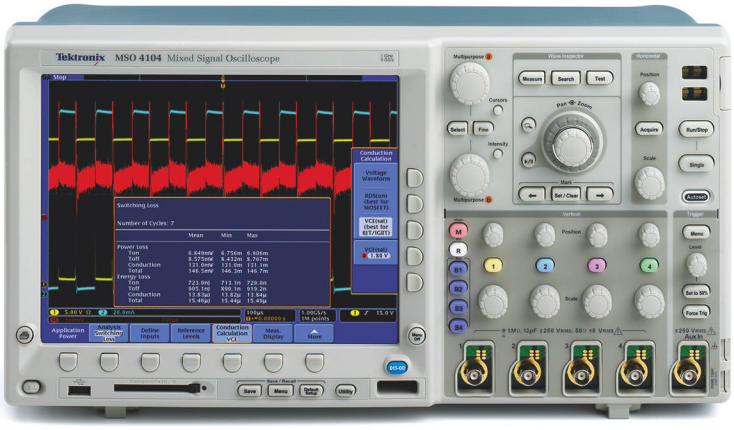
The integrated protocol-specific analysis modules and the host oscilloscopes' Wave Inspector search/navigation tool set and TekVPI (versatile probe interface) combine to transform the scopes into powerful acquisition, display, and analysis tools for rapidly growing market segments and to enhance the productivity of embedded-system developers. You install the modules directly into the oscilloscopes, and they provide one-button automation without the need for special interfaces or external PCs.

The power-analysis module simplifies the probe-deskewing steps that precede power measurements and automates such measurements as power quality, switching loss, harmonic content, SOA (safe operating area), modulation, ripple, and voltage/current-slew rates. One button initiates the tests, and the oscilloscope's screen displays the results. Embedded-system designers who rarely deal with power measurements can obtain the same accurate, repeatable results as power-supply experts.

The audio serial-triggering-and-analysis module provides insight into serial-bus behavior. It decodes and triggers on user-defined packet content and then displays the results as time-correlated waveforms and data packets. The module automatically decodes packet streams in the I²S, LJ (left-justified), RJ (right-justified), and TDM audio-bus formats. Using the oscilloscope's Wave Inspector tools, you can search packet-level content, mark points of interest, and then navigate among these points with the Next and Previous keys and the Pan/Zoom knob.

Both of the new application modules are compatible with the four models in Tektronix's MSO4000 Series, the three models in the DPO4000 Series, and the six models in the DPO3000 Series. US list prices for the DPOxPwr power-measurement-and-analysis module start at $1290, and prices for the DPOxAudio serial-triggering-and-analysis module start at $990. In addition, the manufacturer offers a 25% discount on a bundle that includes—in a hard-sided carrying case—the power module and a selection of power-measurement probes and accessories from the company's broad line.**—by Dan Strassberg**

▷**Tektronix Inc,** www.tektronix.com, www.tektronix.com/power.



Plugging a power-measurement-and-analysis module into this mixed-signal scope—from a series that offers bandwidths to 1 GHz—unlocks capabilities that reside in the instrument's firmware and enables the scope to perform a variety of automated measurements on switch-mode power supplies. A similar module can transform the same scope into a sophisticated debugging tool for several serial-digital-audio buses.

DILBERT By Scott Adams

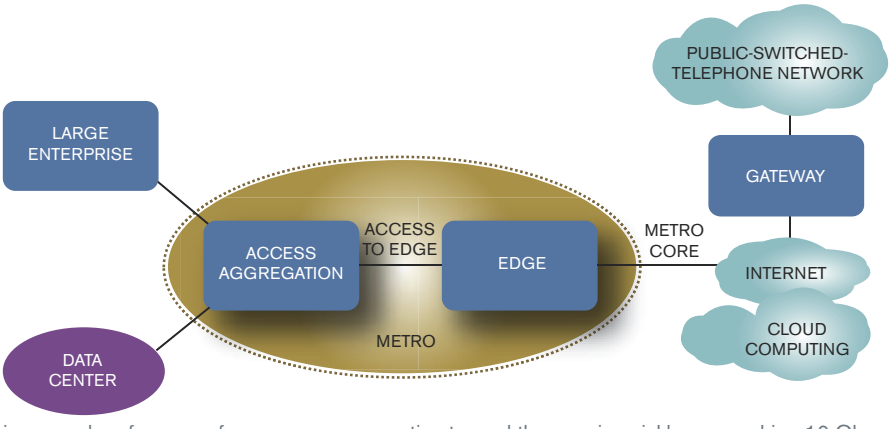
Deploying intelligent networks

Internet traffic is growing exponentially as more and more users employ high-bandwidth applications, such as on-demand, real-time video. As network data rates approach and exceed 10 Gbps, current communications-processing strategies are becoming inadequate. A recent article details plans to enable the deployment of intelligent networks at these high data rates (see "The evolution to network-flow processing: enabling the deployment of intelligent networks at 10 Gbps and beyond," *EDN*, Dec 5, 2008, www.edn.com/article/CA6619896).

According to the article's author, Nabil Damouny of Netronome Systems, with the explosion of Internet traffic, including bandwidth-hungry video, and the ever-increasing need for security, communications equipment must be content- and application-aware at many points in the enterprise and carrier networks. Traditional network-communication processors are inadequate for meeting the requirements at such sustained line speeds. Hence, a heterogeneous multicore, multiprocessing architecture is necessary to meet the performance and power requirements.

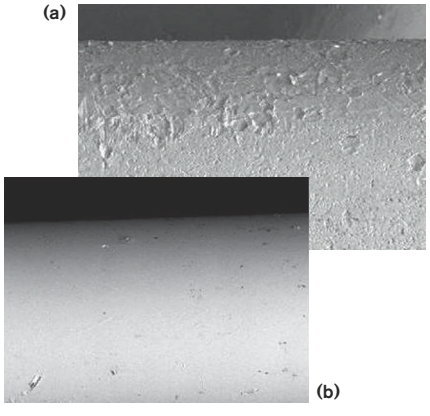
—by Warren Webb

▷**Netronome Systems**, www.netronome.com.



Line-speed performance from access aggregation toward the core is quickly approaching 10 Gbps and beyond.

Bourns hot-dips trimmers to eliminate tin whiskers



A matte-finish tin plating, although ROHS-compliant, can grow dangerously long tin whiskers (a). Bourns' switch to a hot-dipped tin-plated surface on its trimming-potentiometer leads virtually eliminates tin whiskers (b).

Tin whiskers—electrically conductive, crystalline structures that grow from surfaces on which tin is the final finish—have been the bane of electronic products since 2007. During that year, a European ROHS (restriction-of-hazardous-substances) directive essentially banned the use of lead in many electronic devices because tin whiskers can cause short circuits, interference, and unreliability. To virtually eliminate tin whiskers in its trimmers, Bourns' line of ROHS-compliant ceramic-metal-wire-terminal trimming potentiometers now uses a new, hot-dipped tin-plating process. Although the process costs more than the matte-finished leads the company previously used, Bourns is not passing the additional cost on to customers, seeing it as an opportunity to gain market share.

—by Margery Conner

▷**Bourns**, www.bourns.com.

03.05.09

EMBEDDED SWITCH BOOSTS MOBILE COMMUNICATIONS

Targeting rugged, communication-intensive applications in transportation and other mobile-system environments, MEN Micro recently introduced a 3U CPCI (compact-peripheral-component-interconnect)-managed Ethernet switch. The F302 features eight fast-Ethernet channels on the front panel using RJ-45, M12, or D-Sub connectors and an optional channel accessible through the rear J1 connector for fast and secure communications within an embedded system.

The F302 offers an operating temperature of −40 to +85°C and soldered components to resist the effects of shock and vibration. The F302 supports full- and half-duplex, high-speed, nonblocking store-and-forward switching, and autonegotiation as well as Layer 2 switching. Prices start at $987. For more details on this switch, go to www.edn.com/090305pa.

—by Warren Webb

▶MEN Micro, www.menmicro.com.

The F302 switch features eight fast-Ethernet channels on the front panel and an optional channel accessible through the rear J1 connector for fast communications in an embedded system.

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THE EDA TECHNOLOGY LEADER

20-GHz-bandwidth real-time-sampling digital scopes boast new features

Tektronix has announced the high-performance DPO (digital-phosphor-oscilloscope) 70000B and DSA (digital-serial-analyzer) 70000B. Offering the highest four-channel bandwidth in real-time oscilloscopes, the new B models also provide greater ENOB (effective number of bits) than did their predecessors. Adding to the innovative Pinpoint Trigger system, the models also provide hardware-based pattern triggering for advanced serial-data-bus speeds to 5 Gbps.

In addition, new upgrade options through the Tektronix SpeedBooster upgrade program enable users to upgrade their scopes' bandwidth from 4 GHz to 6, 8, 12.5, 16, and 20 GHz. As a result, you are able to minimize your initial investment by purchasing only the instrument bandwidth you need today and can easily increase that bandwidth as test requirements change.

All channels of the DPO/DSA70000B oscilloscopes simultaneously support high bandwidth, deep memory, fast sample rate, and fast waveform capture. You can use the units to debug signals whose data rates are as high as 12 Gbps on each of four lanes. This capability is ideal for use in developing and testing multilane, high-speed serial-data applications, including PCIe (peripheral-component-interconnect-express) 3, 6-Gbps SATA (serial advanced-technology attachment), SuperSpeed USB (universal serial bus), HDMI (high-definition multimedia interface), DisplayPort, and Ethernet.

From the outside, the 70000B-series units appear much the same as their 70000-series predecessors. The new units offer significant improvements in key parameters, such as jitter and vertical noise, and offer attractive new features, such as hardware-based 5-Gbps serial-pattern triggering.

The DPO/DSA70000B oscilloscopes provide scalable performance with 4-, 6-, 8-, 12.5-, 16-, and 20-GHz models. The 20-GHz DSA72004B performs fifth-harmonic measurements on signals carrying data at 8 Gbps and third-harmonic measurements at data rates to 12 Gbps. This performance satisfies the signal-integrity measurement and compliance requirements of the latest third-generation serial-bus architectures. The FastAcq acquisition mode provides a capture rate greater than 300,000 waveforms/sec—about 100 times as fast as competing alternatives—delivering both critical insight into signal behavior and in-depth analysis.

The DPO/DSA70000B Series maximize design margins by providing high signal integrity and fidelity. End-to-end bandwidth from the probe tip to the oscilloscope uses Tektronix TriMode Probes, ensuring signal integrity. With these matching probes, customers obtain full system bandwidth from the probe tip. The units achieve signal fidelity through a low noise floor, flat frequency response, low jitter-measurement floor, and low trigger jitter. Vertical-noise performance has improved over previous models by 1 to 2 dB at all vertical settings.

The DSA70000B models provide hardware-based real-time serial-pattern triggering to 5 Gbps for NRZ (non-return-to-zero) and 8- and 10-bit serial streams. This hardware-trigger capability, along with the Protocol Trigger and Decode application, saves time in debugging and diagnostic work on new high-speed standards by guaranteeing the capture of the first occurrence of a data bus's bit sequence. Some competing approaches use postprocessing to find the pattern after completing the acquisition, requiring many acquisitions to find the desired pattern.

> The P7500 allows users to switch—at the push of a button—between measurements.

The P7500 TriMode probe family now offers performance probes for 4-, 6-, and 8-GHz probes in addition to the previously announced 13-, 16-, and 20-GHz probes. The P7500 Series allows users to quickly and easily switch—at the push of a button—between high-speed-serial differential, single-ended, and common-mode measurements without reconfiguring probe connections to the device under test. All TriMode probes share an expanded set of connectivity accessories, including mobile probing for handheld and fixtured applications; new, high-performance, low-cost, detachable, solder-in connections, which are ideal for probing memory devices; and extended-length, high-temperature probes to address extreme environmental testing.

Tektronix also offers several software packages for high-speed serial-data-link design, debugging, and compliance verification. These packages include DPOJet for jitter and timing analysis; SDLA (serial-data-link analysis) for testing transmitters, interconnects, and receivers; and standard-specific packages for DDR, DisplayPort, PCIe, USB, HDMI, SATA, Ethernet, Fibre Channel, and others. Suggested US list prices begin at $53,300 for the 4-GHz-bandwidth DPO70404B.

—by Dan Strassberg

▷**Tektronix Inc**, www.tektronix.com.

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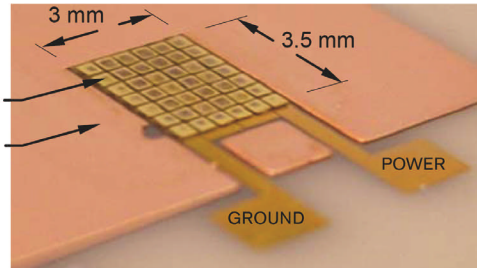


Researchers successfully performed an experiment in spot cooling using a superlattice bismuth-tellurium-antimony-selenium-layered film (courtesy Nextreme Thermal Solutions).

RESEARCH UPDATE

BY RON WILSON

Point cooling advances for hot ICs

Engineers have for years been suggesting using thermoelectric films to cool hot ICs because the films develop a temperature difference between their surfaces when you apply a voltage across them. The problems of getting the film next to the IC, establishing a good thermal connection, and packaging the whole thing in a way that allows the heat to escape have often defeated the undertaking, however. Also, in SOCs (systems on chips) and advanced microprocessors, heat often concentrates in small local areas of the die, so that uniformly cooling the die may be ineffective.

Now, researchers from Intel, Nextreme Thermal Solutions, and RTI International have announced a successful experiment in spot cooling using a bismuth-tellurium-antimony-selenium film. The researchers developed the superlattice film using nanoscale layers of the materials. Attaching the film to the backside of a die, apparently directly under a hot spot in the circuitry, the team was able to then package the assembly in a way that conducted the heat from the film to a conventional heat spreader on top of the package.

The completed assembly was able to cool a 1300W/cm² hot spot by as much as 15°C. The team claims that this experiment is the first successful demonstration of a viable chip-scale-refrigeration technology.

▷**Intel**, www.intel.com.
▷**Nextreme Thermal Solutions**, www.nextremethermal.com.
▷**RTI International**, www.rti.org.

FEEDBACK LOOP

"What appears more likely is that governments will particularly target solar in their stimulus packages with multiple objectives in mind: reducing dependence on foreign energy suppliers, limiting global warming, creating jobs in certain hard-hit areas, and promoting high-tech, clean industries."

—Programmer and *EDN* reader Meredith Poor, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6622867. Add your comments.

RESEARCHERS CREATE SPEEDY, RUGGED CARBON-NANOTUBE MEMORY

03.05.09

Researchers at Helsinki University of Technology have demonstrated that single-walled carbon-nanotube FETs using hafnium-oxide as a gate dielectric can exhibit some of the characteristics of a flash-memory cell, including 100-nsec write/erase times and 10,000-cycle endurance. But the retention time of the devices, 40 hours, is too short for practical application.

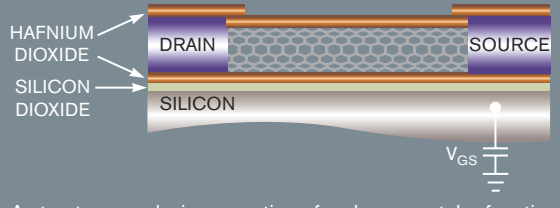
The team fabricated the transistors on a silicon substrate. The researchers used atomic-layer deposition to put a 20-nm layer of hafnium-oxide dielectric over the silicon. Then, the team deposited random segments of nanotubes onto the dielectric layer using a solution containing 1.2- to 1.5-nm-wide, 100- to 360-nm-long nanotubes.

With an atomic-force microscope, the team then identified nanotube segments that settled into the correct orientation for the experiment. The researchers installed palladium source and drain structures on the ends of the selected nanotubes and passivated the assembly's surface with another layer of hafnium-oxide.

The palladium dots act as the source and drain contacts of the transistor, the nanotube is the channel, and the silicon substrate is the gate electrode. Applying a gate-to-source voltage causes charge-trapping in the dielectric layer, influencing the conductivity of the nanotube. The researchers can detect the level of charge-trapping in the transistor by measuring source-to-drain current for an applied source-to-drain voltage.

They can improve the retention time of the device by adding an oxide layer, but they have not yet addressed the problems of accurate placement or proper orientation of nanotubes on the substrate or the variations in nanotube electrical behavior.

▶Helsinki University of Technology, www.tkk.fi.



A structure employing a section of carbon nanotube functions as a memory cell.

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BY HOWARD JOHNSON, PhD

Not your fault

Have you every turned on a light switch, only to see a bright flash just before the whole room plunges into darkness? You just tripped a circuit breaker. That failure scenario requires a light-bulb filament that has almost, but not quite, burned through. When you apply power to the bulb for the last time, a rapid wave of heat stress breaks the filament, sending fragments of broken filament flying around inside the bulb. A short fragment lodges across the power terminals inside the bulb, shorting those terminals together. In that shorted condition, the bulb draws far more current than its designed operating level. The filament shines blindingly white-hot in its last moment before the building circuit breaker pops, disconnecting power to the bulb. This scenario may sound unlikely, but you've probably seen it happen.

In the brief moment before the circuit breaker pops, the power-circuit load comprises three things in series: the hot wire leading to the bulb, the shorted bulb, and one neutral wire coming back (**Figure 1**). In the worst case, a voltmeter touching points A and B could read a voltage drop as high as 60V rms. Under those conditions, the wiring easily dissipates enough power to burst the wiring into flames and toast your whole building. The circuit breaker prevents that scenario.

In addition to circuit breakers, most civilized nations require the use of modern, three-pronged grounding outlets. In that application, only the hot and neutral wires carry power currents. The green safety wire, or "third wire," merely connects the metallic chassis of each product to earth at the ac power entrance. Under ideal, no-fault conditions, the green safety wire carries no current. An inexperienced designer might therefore conclude that the green wires form a single-point-ground reference system that provides a consistent voltage reference between different ac-powered products. It does not serve that function (**Figure 2**).

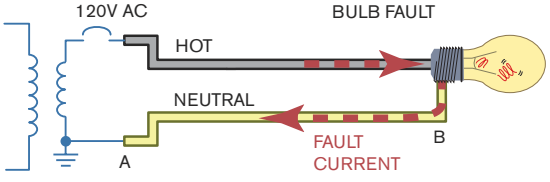


Figure 1 A broken filament creates a short circuit.

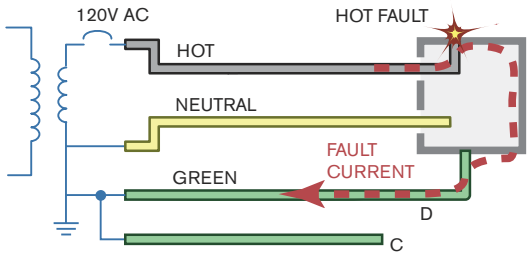


Figure 2 The green wires prevent the faulty chassis from remaining energized but do not prevent large voltages from appearing between points C and D.

The box on the right represents an old vending machine with a metal body. One day, a hot wire inside the machine accidentally breaks free. It touches the metallic chassis, creating a potentially dangerous situation. Immediately, the product's green safety wire conveys a large fault current back to the power source. That action is the sole function of the green wire. The fault current trips the circuit breaker, shutting off power and possibly saving the life of the next person who wants a candy bar.

As the fault current surges through the green wire, other products plugged into the green-wire system at adjacent outlets C and D could experience voltage differences as large as 60V rms. Even though the original fault lies within the vending machine, if the surge blows out your equipment, you inherit all the blame. It would be better if you design gear that can sustain such extraordinary voltages without damage.

Suitable architectures for interchassis data transfer that can easily sustain 60V rms without disruption include well-balanced, transformer-isolated standards, such as Ethernet; fiber-based optical links; free-space IR (infrared) optics; and RF transceivers. You should use interfaces such as RS-422 that lack large common-mode immunity only between equipment that permanently connects to a common outlet or power strip. EDN

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

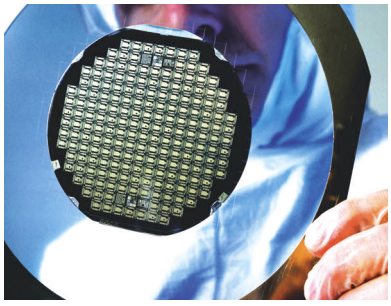
Mitigating tapeout risk

The last few process-technology nodes emerged after major shifts in technical and physical complexity and rising manufacturing costs. During these shifts, chip-design teams have had the constant availability of expert personnel, design tools, and computing/IT resources that were sufficient to complete the projects. Recent economic conditions, however, have eroded the availability of these infrastructure resources.

Most physical-design engineers focus on the performance aspects of the design rather than the whole flow. Downsizing or divisional restructuring, however, quickly disrupts the sign-off loop for a design release. Most companies have a manual sign-off-review process during which experts from design engineering, physical design, and manufacturing/operations review the physical design and design verification and determine whether the product is ready for release. Some of these personnel are familiar with the project. Companies must capture the knowledge of these key people and incorporate it into an automated sign-off-release procedure.

One of the biggest issues is the availability of a manufacturing-knowledgeable staff to participate in this review. The in-house-wafer-fab business model has in-house expertise for this manufacturing interface. Most companies have lost this resource, however, because they use wafer foundries as their suppliers. To minimize risk, companies should now include the foundries' technical representatives in the results-review portion of the release procedure. Including these people avoids the need for multiple sign-off cycles after the receipt of the design data and before the start of manufacturing. The

Companies should now include the foundries' technical representatives in the results-review portion of the release procedure.



companies should make these foundries partners in the flow rather than hold them at a distance as they would subcontractors or suppliers.

Restructuring at many semiconductor-design groups has resulted in a large reliance on reuse of known-good blocks in new designs. When the designer originally responsible for the blocks is available, this method is known and proven and reduces risk. Loss of the oversight of the original designers orphans a great deal of the data for these blocks, leaving design data without context. Without that context, reusing this data in another application is risky. Doing design-application checking and statistical sensitivity analysis in the physical-verification portion of the design can reduce this risk. Several new software tools from such companies as Mentor Graphics (www.mentor.com) and Solido Design Automation (www.solidodesign.com) address this market.

Current process technology at the 65-, 45-, and 40-nm nodes has a high cost of manufacturing and requires large design teams to effectively use the many available devices. Most applications do not require huge numbers of devices, however. Also, many function blocks—standard interfaces such as SATA (serial advanced technology attachment), 802.11, USB (universal serial bus), and HDMI (high-definition multimedia interface)—also have known, tested, and validated intellectual property in older process technologies, such as 250, 180, 150, 130, and 90 nm. So, you can both offset a great deal of risk and save money by targeting these older process-technology nodes. These older nodes also have the advantage of well-defined flows and stable software tools.

One easy-to-implement factor for reducing risk on a new tapeout is to increase the number of available power and ground pairs. Designs with lower power-supply voltages and multiple power modes have lower PSRRs (power-supply-rejection ratios) and higher noise floors. Adding power and ground pairs and creating power and ground islands help minimize and isolate the noise. An added benefit is that you can more finely tailor testing and debugging as the increased power resources minimize interdependencies among the blocks. EDN

Contact me at pallabc@siliconmap.net.

www.edn.com/tapeout

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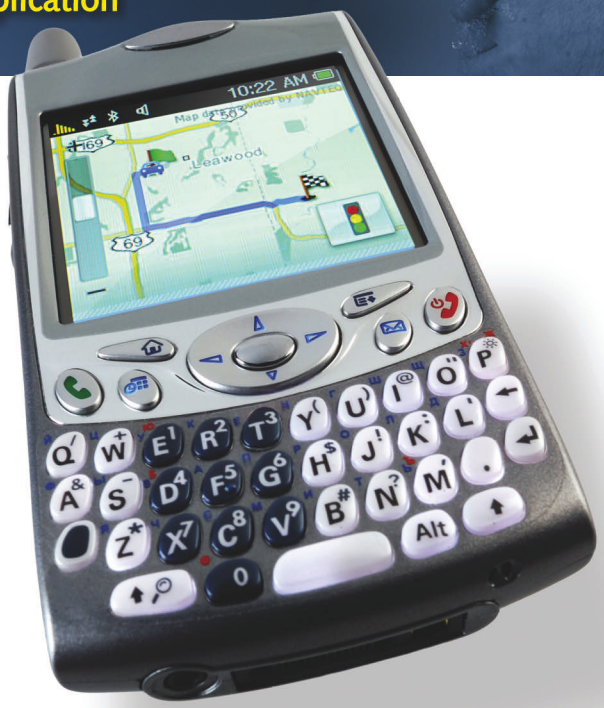

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Integration Makes Life Easier

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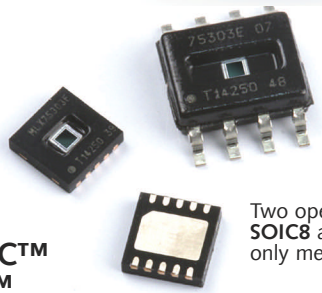

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INTO THE MAINSTREAM

BY GRAHAM CELINE, AZIMUTH SYSTEMS • SANDY FRASER, AGILENT TECHNOLOGIES

The universal demand for constant access to voice and data communication, along with the increasingly rich availability of Wi-Fi (wireless-fidelity) and cellular connectivity, is driving a widespread demand for converged Wi-Fi/cellular applications and services. Promising better access to voice and data services as well as lower communication costs, FMC (fixed/mobile convergence) has the potential to greatly affect the world of communications.

Before FMC technology can truly take off, however, it is critical for wireless-IP (Internet Protocol) networks and 802.11a/b/g/n devices to deliver the same underlying quality of service as their cellular counterparts. As users move within Wi-Fi networks, as well as between Wi-Fi and cellular networks, FMC must deliver a satisfying end-user experience, featuring good voice quality, few dropped calls, reliable and high-throughput data connectivity, long handset-battery life in standby and active states, and seamless voice and data roaming and handoff. These user-experience metrics see direct influence from Wi-Fi statistics that define mobility performances such as range, roaming, and hand-in/handout capability.

For mobility-performance testing to be effective from quality, coverage, and cost perspectives, the test method must accurately re-create the real world in an efficient, repeatable, cost-effective, and scalable manner. As a result, an inte-

grated testing approach that allows engineers to evaluate the performance of their converged devices and networks from both the Wi-Fi and the cellular perspectives is necessary.

THE ABCs OF FMC

With its promise to seamlessly deliver quality fixed services and applications, including voice, video, and data over mobile wireless networks to handsets or endpoint devices, FMC represents a large commercial opportunity for infrastructure vendors to deliver back-end integration products and services, as well as for service providers to generate additional revenue from cellular-network-infrastructure investments, Wi-Fi approaches, or both. Despite this market opportunity, the industry has yet to deliver compelling FMC applications and services for end-user adoption. To drive such broad market acceptance, it's critical for infrastructure vendors and service providers to capitalize on the major benefit that FMC provides: the convenience of having one device and phone number for both mobile networks and corporate or home networks.

Using a voice call that the cellular network seamlessly transfers to the corporate or home network, users can enjoy continuous communication and benefit from improved coverage of the Wi-Fi network and reduce cellular-minute usage as a result of the call's moving off the cellular network. Alternatively, moving voice calls from a corporate or a home network to a cellular network enables continuous communication when users leave their office buildings or homes. The ability to use data applications where and when users want will also enable significant improvements in personal and professional productivity. While users are stationary or mobile in locations that a cellular or Wi-Fi network covers, they will have access to Internet-based applications such as e-mail, Web browsing, and online services, representing a huge draw for potential users of FMC services.

Beyond the importance of seamless voice and data communication, the ability to provide cost savings that are not available from alternative Wi-Fi and cellular-only services, as well as a satisfying end-user experience, drive sustainable consumer demand for FMC services. Cellular services have established user-experience expectations that new converged services must meet or exceed. Failure to deliver a satisfying end-user experience will provide consumers with little motivation to adopt converged Wi-Fi-plus-cellular services, resulting in an industry that cannot generate sustainable demand for FMC services.

AT A GLANCE

- FMC (fixed/mobile-convergence) technology can not take off until wireless-network and 802.11 devices deliver the same quality as their cellular counterparts.
- Vendors and service providers must capitalize on the major benefit of FMC: the ability to have one device and phone number for both mobile networks and corporate or home networks.
- It requires extensive testing to prove that the network efficiently conducts Wi-Fi (wireless-fidelity) roaming sufficient to maintain data throughput, voice quality, and call continuity.
- Engineering efficient Wi-Fi-to-cellular handovers requires complex changes to the back-end cellular network and to decision-making algorithms.

USAGE SCENARIOS

The primary driver of the growth in consumer demand for long-range cellular-network services has been improvements in mobile voice services and value-added data services, such as text messaging, e-mail, and Web access. FMC broadens the range of this capability by taking advantage of Wi-Fi technology indoors, where cellular coverage may be less reliable. Although moving coverage onto the Wi-Fi network provides users with access to potentially much faster services, it is critical that this Wi-Fi connectivity also sustains mobility and quality of service.

Converged Wi-Fi-plus-cellular services must also support the same or better quality of voice and data services while the user is in motion and transferring the networks. Mobility services require adequate performance in Wi-Fi range, Wi-Fi roaming, and hand-in/handout network transfers.

Wi-Fi range, the perceived quality of voice and data services as users move closer to and away from a Wi-Fi AP (access point), is a significant measure of Wi-Fi performance. Unlike cellular technology, Wi-Fi technology varies the transmission data rate to minimize packet errors. A Wi-Fi transmitter on the AP or the client uses dynamic-rate-adaptation algorithms to control the transmission data rate on a packet-by-packet basis. These algorithms consider many network and environmental variables, including received-signal strength and packet-error rate, in deciding to increase or decrease the transmission rate. If the implementation is poor, the movement of a user around a Wi-Fi AP will significantly affect the data

TABLE 1 TYPICAL MOBILE-PERFORMANCE SCENARIOS

User-experience scenarios	Mobile-performance scenarios
Using a Wi-Fi game controller while playing a console video game	Data throughput over range
Walking around a house while on a voice-over-Wi-Fi call	Voice quality over range
Downloading a new release of a band to a portable music player while walking around the airport	Data throughput during AP-to-AP roaming
Making a voice-over-Wi-Fi call between an office and a conference room	Voice quality and dropped calls during AP-to-AP roaming
Making a conference call while heading into the office	Voice quality and dropped calls during hand-in/hand-out network transfer
Making microwaved popcorn causes dropped calls	Interference from microwave oven
Experiencing more battery drain at home than at work when using Wi-Fi	Battery life over various network conditions

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throughput and voice quality that the user experiences. Proving that the rate-adaptation algorithms are implemented properly requires extensive range testing of the client and AP devices.

Wi-Fi roaming, the ability to provide quality voice and data services while the user is moving between Wi-Fi APs, is another critical measure of Wi-Fi-device performance. Both cellular and Wi-Fi networks use algorithms to transfer connectivity from one infrastructure device, such as a cellular base station or Wi-Fi AP, to another as connection conditions require. Cellular networks use roaming algorithms on the base station, which the network manages, to make roaming decisions in consideration of real-time network conditions, such as base-station loading and base-station-service outage. In contrast, Wi-Fi networks use roaming algorithms on the client, which makes roaming decisions without considering real-time-network conditions. This difference means that Wi-Fi clients could decide to roam to an AP that is overloaded or functioning improperly, resulting in significantly reduced data throughput and voice quality or a session's termination.

In addition to the differences in the implementation of the roaming algorithm, cellular and Wi-Fi networks execute roaming through different means. When a voice call is in progress, cellular networks execute roaming using a make-before-break approach that establishes the connection between the handset and the base station that gains control of the session before terminating the connection between the handset and the base station that is giving up control of the session. Depending on network setup, data services over cellular networks can use either make-before-break or break-before-make approaches.

EXTENSIVE TESTING IS IMPORTANT TO VALIDATING THE IMPACT OF HANDOVER ON THROUGHPUT, VOICE QUALITY, AND CALL CONTINUITY.

Wi-Fi clients, however, always execute roaming with a break-before-make approach in which the client terminates connectivity with one AP before establishing connectivity with a new AP. A poorly implemented roaming algorithm on the client can result in a significant delay before establishing the connection with the new AP or even failure to make the connection. These issues can severely affect data throughput, voice quality, and call continuity.

Transferring session connectivity between Wi-Fi and cellular networks, a hand-in/handout transfer, is even more complex than a Wi-Fi-to-Wi-Fi roam or a cellular-to-cellular handover. In the case of voice calls, this Wi-Fi-to-cellular transition is always make before break, adding complexity to the normally simple Wi-Fi-to-Wi-Fi transition. With the differences between cellular and Wi-Fi-handover and roaming-algorithm implementations, engineering efficient Wi-Fi-to-cellular handovers requires complex changes to the back-end cellular network, as well as significant changes to decision-making algorithms. With this increased complexity, extensive testing is important to validating the impact of handover on throughput, voice quality, and call continuity.

TABLE 2 REQUIRED WI-FI-MOBILITY-PERFORMANCE TESTS

Mobile-performance scenario	Wi-Fi-performance metric	Wi-Fi-performance test
Data throughput over range	Data rate, packet loss, error rate	Throughput in megabits per second as a function of distance from a Wi-FI AP—the position of your office relative to AP, for example
Voice quality over range	Packet loss	Voice quality measurement—PESQ (perceptual-evaluation-of-speech-quality)-based scores—as a function of distance from the Wi-Fi AP, such as talking on the phone in front of the TV or in the kitchen
Data AP roaming	Roaming time, data rate	Roaming time in seconds for failover roam as a handset moves to a new AP because one has failed, such as during a power glitch or network failure; roaming times for smooth roaming as a handset moves between two Wi-Fi APs, such as during walking between work areas
Voice-over-Wi-Fi handover	Roaming time, packet loss, error rate	Number and percentage of voice calls dropped as handset moves between two Wi-Fi APs or transfers from Wi-Fi to cellular networks and vice versa, walking to another part of a building while talking on the phone or moving outside the building; voice-quality measurements—PESQ-based scores when handset moves between two APs or transfers from Wi-Fi to cellular networks and vice versa, such as maintaining call quality when moving around a house or when moving from a garden into a house

REAL-WORLD WI-FI MOBILITY

Unlike cellular networks, which are the sole occupiers of the licensed-RF spectrum in which they operate, a Wi-Fi network operates in unlicensed spectrum that it shares not only with other Wi-Fi networks, but also, potentially, with other RF networks, such as Bluetooth—or even with other RF devices, such as cordless phones and microwave ovens. As a result, when discussing the performance of FMC devices employing Wi-Fi, the impact of the real-world-environment conditions in which the devices operate also requires recognition.

In addition to the RF interference that Wi-Fi networks and RF devices competing for spectrum create, solid obstacles, such as walls and furniture, as well as the movement of objects, such as vehicles, can create RF-signal conditions—multipath and fading—that affect the performance of Wi-Fi devices. Most FMC approaches use a nondedicated IP network as a primary carrier of

the voice data, which can directly affect voice quality as traffic load varies. As a result, to maintain the best possible FMC services, converged Wi-Fi-plus-cellular handsets must deliver the best Wi-Fi-mobility performance in all of these real-world conditions.

To determine the impact of Wi-Fi performance on user experience, it is important to first identify the critical mobile-performance scenarios that directly affect the user (**Table 1**). These mobile-performance scenarios establish the fundamental Wi-Fi-performance metrics, including data rate, packet loss, error rate, and roaming time, that require testing. You can then develop a set of essential tests for the evaluation of the Wi-Fi-mobility performance (**Table 2**).

An integrated approach to testing FMC devices and networks must feature parametric measurement plus flexible protocol and triggering analysis and emulation of a network with full connectivity to the Internet. By providing an emulated generic-access network, such an approach enables engineers to test the conformance and functions on the GSM (global-system-for-mobile)-communications side, as well as the handover reliability between the generic-access and GSM networks.

METHOD FOR TESTING

OTA (over-the-air) testing, in which engineers test device performance by replicating the conditions of the environments in which the device will operate, is one common method of evaluating Wi-Fi-mobility performance. OTA testing relies on empty office buildings, homes, and live networks to accomplish its goals. OTA tests for mobility and roaming use mobile carts, moving Wi-Fi and cellular equipment to various locations in the test space and manually configuring tests and recording test results at each location.

Because this approach depends largely on the uncontrollable nature of OTA environmental conditions, engineeers manually perform most testing. As a result, several critical factors limit the effectiveness of Wi-Fi-mobility-performance testing using OTA methods. The time-consuming manual test setup and execution typical of OTA tests limit the ability of this testing method to scale. Consistent, repeatable test measurements are also nearly impossible in OTA environments, thereby limiting the ability to reliably repeat the tests in the future. In addition, RF interference may vary with each test iteration, even at the same location, possibly making it impossible to reproduce results and issues.

DEVICE ISOLATION REPLICATES THE WI-FI NETWORK IN A CONTROLLED, CABLED ENVIRONMENT.

The alternative to OTA testing is testing in a controlled RF environment, through approaches such as room isolation, which places the Wi-Fi-test setup in a screen room that filters out external RF interference. Due to the large installation and maintenance costs of the screen rooms, room isolation is costly. Additionally, the size of the screen room severely limits the effectiveness of testing distance, roaming, and mobility performance. Device isolation is a more advanced method of controlled RF testing, in which you place all testbed devices in individual isolated enclosures and connect them with cables to programmable RF attenuators, combiners, and switches. This test method replicates the Wi-Fi network in a controlled, cabled environment that stabilizes the RF connection by removing the variability of OTA systems.

Unlike other testing approaches, device isolation features a controllable testbed with numerous benefits. Isolation of devices under test from external RF interference provides a controllable RF environment to conduct repeatable mobility testing. By using a controlled, cabled RF environment, such testing approaches reduce costs by eliminating the need to design, build, and maintain homegrown testbeds and costly RF screen rooms. Other benefits of this test method include the programmable tes-

tbed and tools that enable automated test configuration and execution. Users can automatically configure any network device and dynamically position any network node to analyze the effect of mobility on both device and network performance. Additionally, automated test configuration allows for simple, effective setup and reuse. Using programming, you can create scripts that require little human intervention and can automatically run multiple iterations of configurations in a fraction of the time it takes for manual testing. This repeatability reduces the time you spend on the quality assurance and benchmark-test processes and, as a result, dramatically reduces time to market and testing costs.

Test scalability is an additional important benefit of the device-isolation approach. If you properly build the controlled RF environment, you can scale Wi-Fi testing from a single device to the entire network. Users can configure an entire Wi-Fi network and provide system-level testing of actual APs, clients, and other wireless devices. You can test networks under a variety of traffic- and client-load conditions. Client- and traffic-load emulation enables the development of test setups that re-create a busy network environment for the devices under test. This approach provides the ability to test Wi-Fi-mobility performance in controlled conditions. By using this test approach, engineers can assess the impact of one or a combination of conditions, including RF multipath and fading, background Wi-Fi traffic, RF interference, and IP-network delay, on the mobility performance of 802.11a/b/g/n devices.

FMC developers, users, and service providers have a variety of testing requirements they can address with device isolation, ranging from a development environment in which controlled isolation in a crowded RF lab can be invaluable to integration. System-engineering groups within service-provider organizations conduct another critical test process. They use these same test scenarios to validate interoperability of devices from different suppliers, to benchmark the performance of different configurations to make purchasing decisions, and to certify devices for deployment. For the engineers who select FMC handsets that will operate on service-provider networks, effective performance benchmarking provides a means of performing an apples-to-apples comparison of the Wi-Fi-mobility performance of FMC handsets. EDN

AUTHORS' BIOGRAPHIES

Graham Celine is senior director of marketing at Azimuth Systems. He has 20 years of high-tech experience, having joined Azimuth after a 13-year career in data networking. He has a bachelor's degree in electrical engineering from the University of Witwatersrand (Johannesburg, South Africa).

Sandy Fraser is the mobile-broadband-division product manager for Agilent Technologies. Fraser is responsible for GSM, GPRS (general-packet-radio service), and EGPRS (enhanced GPRS) R&D test products.

BY ROBERT CRAVOTTA ○ TECHNICAL EDITOR

THE 2009 DSP DIRECTORY

DIG INTO DSPs

THIS REPOSITORY OF EMBEDDED-SIGNAL-PROCESSING RESOURCES WILL HELP YOU FIND THE BEST PROCESSOR CANDIDATES AND DEVELOPMENT TOOLS FOR YOUR PROJECT.

WELCOME to the 2009 *EDN* DSP Directory. As in previous years, the directory provides a snapshot of the companies, products, and tools available as digital-signal-processing resources for embedded-system developers. The number of companies, devices, cores, and offerings in the directory continues to grow. Some product lines have dropped off the list only to be replaced by new ones. *EDN* is constantly uncovering companies that previous editions of the directory did not list. If you notice a company that we omitted, please let the company and us know that you would like to see it in the next update of the directory.

The print version of this directory is but a small fraction of the entire directory that stresses what is new over the last year for each company. Visiting the Web version of this directory at www.edn.com/dspdirectory has taken on more importance as the company roster continues to expand the material well beyond the capacity of the print update. The directory lists the companies selling software-programmable processors, cores, and software-development resources; provides an overview for each; and identifies the latest developments over the previous year at each company.

This directory aims to provide designers and system architects enough visibility to dig into the processor options and quickly narrow the list of candidate processors for their project. The expanded online section presents each processor with detailed information and block diagrams. The directory uses a common taxonomy for describing and categorizing target applications that helps you to quickly find and compare competing processors for your projects. The Web material has more details on the common application taxonomy so that you can comment on it and we can refine it as appropriate.

The "Where are they now?" sidebar on the Web helps you find companies that we no longer list, whether because they closed their doors, they changed their focus, another company acquired them (think AMI Semiconductor), or they spun off into another company. As always, the Web site duplicates and greatly expands upon the material you find in the print version.

If this directory helps you find or choose a device or core, please let the vendor know how you found its part. Help us continue to improve the directory by visiting us at www.edn.com/dspdirectory or by sending your comments and feedback to dspdirectory@edn.com.

ACTEL
WWW.ACTEL.COM

Actel offers single-chip-, nonvolatile-FPGA technologies along with signal-processing capabilities, such as filtering and domain conversion. The company's DirectCore system-level IP (intellectual-property) blocks target use with its FPGAs, such as the RTAX-S and ProASIC3 device families. When you implement the flexible IP cores in Actel's flash- and antifuse-based FPGAs, they are immune to firm errors and tolerant of radiation. The company's devices support live-at-power-up capability, which allows them to target military, communication, aerospace, and medical applications that require no power-up delay.

ALTERA
WWW.ALTERA.COM

Altera's portfolio of FPGAs, structured ASICs, and CPLD products targets many electronics markets. Building on the Stratix device family, the 65-nm Stratix III FPGAs incorporate dedicated DSP blocks to combine high performance with the lowest possible static- and dynamic-power consumption; these new devices improve performance by as much as 50% over previous-generation high-end FPGAs devices. Stratix III FPGAs features include Programmable Power Technology, selectable core voltage, process and circuit technologies, and support from the Quartus II PowerPlay power-analysis and -optimization technology. The 65-nm Cyclone III FPGAs with 288 embedded multipliers for DSP applications target high-volume applications requiring low power, high performance, and low cost. HardCopy II devices give volume-driven-application designers the ability to seamlessly migrate their design from a high-end Stratix-series FPGA to a low-cost structured-ASIC product. The company offers a library of IP cores, including the Nios II embedded processor. The Quartus II design software supports all Altera products for FPGA, structured-ASIC, and CPLD designs.

ANALOG DEVICES
WWW.ANALOG.COM

Analog Devices' DSP offerings include the Blackfin, SHARC, and TigerSHARC families of processors. Development tools for all of the company's processors include VisualDSP++, VisualAudio, and Ez-Kit Lite, as well as tools from SigmaStudio, µClinux, and Green Hills Software. The Blackfin-processor family combines a 32-bit RISC-like instruction set with 16-bit dual MAC (multiply/accumulate) units and targets convergent applications with audio-, video-, and data-processing requirements. The devices' dynamic-power management enables lower power consumption by supporting the simultaneous adjustment of system operating frequency and voltage under application control.

The SHARC-processor family targets applications ranging from consumer, automotive, and professional audio to industrial, test and measurement, and medical equipment. The 32-bit floating/fixed-point core architecture includes a sophisticated memory and I/O-processing subsystem. The TigerSHARC-processor family offers high floating-point and fixed-point performance and high-density performance. It supports glueless-multiprocessor scalability targeting wireless-communications-infrastructure, medical-imaging, industrial-imaging, and military applications.

Analog Devices' SigmaDSP audio processors provide a single-chip audio system with a 28/56-bit audio DSP, ADCs, DACs, and microcontroller-like control interfaces. Signal-processing elements include equalization, crossover, bass enhancement, multiband dynamics processing, delay compensation, speaker compensation, and stereo-image widening, which you can use to compensate for the real-world limitations of speakers, amplifiers, and listening environments.

ARC INTERNATIONAL
WWW.ARC.COM

ARC licenses consumer IP (intellectual property) in the form of vertically integrated products, multimedia subsystems, configurable processors, and related technologies to semiconductor and OEM companies worldwide. These ARC products enable designers to create consumer-electronics products that deliver an enhanced multimedia experience on products such as DTVs, portable media players, PCs, laptops, and music and smart phones. ARC's new Sound-to-Silicon products comprise ARC's audio-enrichment software; low-power hardware platform, including ARC XY Advanced DSP Memory subsystem and ARC 600 family core; codecs and related software; and development and mastering tools and services.

For semiconductor companies, the Sonic Focus ready ARC Sound Subsystem offers low power and small form factors. Codecs, drivers, operating systems, and software-development and EDA tools complement the configurable ARC processor in the subsystem. By leveraging the configurable nature of the ARC Sound Subsystem in combination with the scalable Sonic Focus audio IP, developers can design a platform to target multiple audio applications.

ARC's Sonic Focus software consists of an acoustical-modeling and time-domain-analysis engine. Optimized for the low-power ARC Sound Subsystem, it delivers a natural listening experience and extends playback time on battery-powered products. OEMs can choose from multiple silicon suppliers offering ARC-based chips for their devices.

ARM
WWW.ARM.COM

ARM licenses semiconductor IP (intellectual property), including processors, peripherals, interconnect, and physical libraries for the development of complex SOC (system-on-chip) devices. ARM processors target automotive, consumer-entertainment, imaging, networking, storage, security, and wireless applications, and ARM bases them on a common architecture that emphasizes performance, low power consumption, and reduced system cost. The company offers a range of processor cores, including the ARM7, ARM9, ARM10, and ARM11, as well as the Cortex family of processors featuring Thumb-2 technology and the SecureCore-processor family. ARM's DSP-enhanced cores support products that require a mixture of DSP and control functions on a single core. ARM Neon technology provides powerful, flexible acceleration for media and DSP applications; ARM OptimoDE Data Engine technology targets power-efficient, deeply embedded signal-processing applications; and the ARM9E processor family is well-suited for products for microcontroller-DSP and Java applications.

ATMEL
WWW.ATMEL.COM

Atmel bases its DSCs (digital-signal controllers) on its proprietary AVR32-UC3 and AVR32-AP7 cores and on ARM's ARM926EJ-S core. The company's Diopsis families of dual-core, VLIW (very-long-instruction-word), floating-point DSPs include its complex-domain GFLOPS Magic core with ARM7- or ARM9-based microcontrollers.

Atmel's newest 32-bit DSC family, the AVR32-UC3B, offers 12-Mbps USB 2.0 OTG (On-The-Go) and is suitable for PC-centric, USB-enabled applications, such as flash disks, pointing devices, printers, and USB-ready embedded-system applications. The UC3B offers true single-cycle execution of MACs (multiply/accumulate) instructions and DSP arithmetic and delivers 72 DMIPS at 60 MHz and 23 mA at 3.3V. Standby-power consumption is less than 10 µA with 1.8V/3.3V dual power supplies.

Atmel's AVR32- and ARM-based DSCs use the same peripheral set, which includes DMA on all peripherals, Atmel's peripheral DMA controller, multilayer high-speed-bus architecture, Ethernet MAC (media-access controller), USB host/device, ADC, and serial-communication peripherals, as well as an optional external-bus interface. Atmel's Cap customizable microcontroller, which it based on the ARM processor, additionally provides a large block of digital logic that application developers can customize to include a DSP coprocessor.

AUSTRIAMICROSYSTEMS
WWW.AUSTRIAMICROSYSTEMS.COM

Austriamcrosystems bases its high-performance analog ICs on more than 25 years of analog-design and system know-how with its own state-of-the-art manufacturing and test facilities. The company leverages customized and standard analog products focusing on power management, sensors and sensor interfaces, and portable audio. The flexible and fully integrated AS3525 audio-processor system uses a 200-MIPS ARM9TDMI core; it can perform MP3, AAC (advanced audio coding), AAC+, WMA (Windows media audio), and Ogg, and it can support extensive user interfaces, motion graphics support, and video playback. Large on-chip RAM leads to power consumption of 58 mW for a complete flash-based MP3 player.

CAMBRIDGE CONSULTANTS
WWW.CAMBRIDGECONSULTANTS.COM

Cambridge Consultants' expertise covers semiconductors, wireless communications, radar systems, advanced sensors, and control systems in automotive electronics, medical devices, and consumer goods. The company's IC-design capabilities include high-precision analog-mixed-signal and RF products.

The company's portfolio of IP (intellectual-property) and development tools includes an extensive library of analog, digital, mixed-signal, and wireless-IP cores together with embedded software-development and debugging tools, protocol stacks, and design platforms for ASICs and FPGAs. The IP cores are portable and flexible, and designers can tailor them to their specifications with flexible licensing contracts that can be royalty-free. Cambridge Consultants' silicon-IP offering includes 16- and 32-bit XAP processor cores and the APE2 configurable-datapath DSP.

CEVA
WWW.CEVA-DSP.COM

Ceva licenses a family of synthesizable, programmable DSP cores, DSP-based subsystems, and application-specific platforms, including multimedia, audio, VOIP (voice over Internet Protocol), Bluetooth, and Serial ATA (advanced technology attachment). The Ceva-X DSP architecture supports features and capabilities for advanced signal-processing requirements, including 3G/3.5G/WiMax/LTE (long-term evolution) baseband, video, audio, and VOIP processing. Ceva hardware- and software-development tools provide support for all of Ceva's DSP cores and system platforms, as does Cevanet technology partners, which provide application software, RTOS implementations, simulation tools, and EDA tools.

In 2008, the company's customers shipped more than 300 million Ceva-powered chip sets, an increase of 25% over 2007 shipments. During the year, the company launched the Ceva-HD-Audio DSP Platform, which it based on the high-performance 32-bit Ceva-TeakLite-III DSP core running at speeds as high as 550 MHz. The Ceva-HD-Audio's HD-audio codecs support two to 7.1 channels with various bit rates and support the leading audio standards. The company also enhanced its Ceva-X family of DSP cores, introducing the Ceva XS-1100A for wireless-baseband applications, and the Ceva XS-1200A, which targets multimedia and other applications requiring high-performance signal processing. Ceva continued to move into China with design wins and support for local standards. The company collaborated with NBICC to add China's AVS (Advanced Video System) video standard to Ceva's MM2000 platform and HuaXun to deliver a software-GPS (global-positioning-system) product for Ceva-X DSP cores and the MM2000 multimedia platform. Ceva strengthened the ecosystem of support around its DSP product, partnering with ARM to better facilitate SOC (system-on-chip) designs.

CHIPWRIGHTS
WWW.CHIPWRIGHTS.COM

Fabless-semiconductor company Chipwrights offers DSPs and SOCs (systems on chips) for audio-, video-, and image-processing applications. The Chipwrights processor family combines a 32-bit, RISC-like serial application processor with an array of 32-bit MAC (multiply/accumulate), ALU (arithmetic-logic-unit), and shift parallel processors. The parallel scalable architecture enables it to process more data than conventional single/dual-core devices with fewer cycles and less power consumption.

The company offers turnkey options for IPTV (Internet Protocol television) and IP cameras, including an evaluation board; system software; the Linux 2.6 operating system; the Eclipse IDE (integrated development environment); FFMpeg; the QT library; a Webkit-based browser; and a comprehensive audio/video/image library, including MPEG, JPEG, REAL (remote electronic access for libraries), Win Media, dewarping, image filters, and color filters. Use the IPTV turnkey product to develop video-decoding applications, such as IP-Card for TV, PMP (portable media player), navigation, and PDA (personal digital assistant). The IP-Camera turnkey product is useful for developing any camera application, such as CCTV (closed-circuit television), Web, and conference-room cameras. In addition to turnkey products, the company offers a media-development kit for developing any audio/video application.

Last year, Chipwrights introduced CW5631, which combines an ARM926EJ-S processor with 16 32-bit parallel processors and a serial application RISC processor, enhanced video-I/O ports, high-speed USB, I²S/AC97 (inter-IC-sound/audio-codec-97) audio, Compact Flash, 10/100-Mbps Ethernet interface, and Secure Digital/MMC (multimedia-card) interfaces.

CIRRUS LOGIC
WWW.CIRRUS.COM

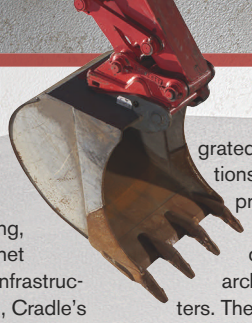
Cirrus Logic develops high-precision analog- and mixed-signal ICs for consumer and energy-related markets. Cirrus Logic DSPs target audio applications and feature an extensive library of audio-processing algorithms for feature differentiation. New in 2008 was the CS47048, an innovative, eight-channel audio DSP with an integrated mixed-signal codec, S/PDIF (Sony/Philips digital-interface-format) receiver, and sample-rate converter, complete with a graphical software-development tool, for automotive-audio applications. Cirrus will introduce in 2009 this flagship DSP/mixed-signal product and similar products for home-entertainment applications. The company also introduced stereo and multichannel-audio DSPs offering audio volume-leveling-enhancement software, such as Dolby Volume, SRS Labs' TruVolume, and Audyssey Labs' Audyssey Dynamic Volume.

NEW COREWORKS
WWW.COREWORKS-SA.COM

Coreworks, a vendor of licensable silicon IP (intellectual property), recently developed SideWorks. The DSP technology targets cost- and power-sensitive applications, such as multimedia and communications. SideWorks enables the creation of DSP cores that are both configurable before fabrication and reconfigurable. The movement of data and some aspects of the execution-unit function are programmable at runtime. SideWorks does not run as a stand-alone processor; it combines with a general-purpose host processor that manages program flow and data I/O. Therefore, Coreworks also supplies FireWorks, a compact, 32-bit RISC-CPU core. Coreworks' initial business model is to license fully preconfigured standard IP modules based on the SideWorks architecture and to create SideWorks instances for customer-specific needs. A SideWorks Mixed-Radix FFT (fast-Fourier-transform) module is available, and modules targeting digital audio, including Dolby Digital and AAC (advanced audio coding), are under development.

CRADLE TECHNOLOGIES
WWW.CRADLE.COM

Fabless-semiconductor company Cradle Technologies develops multicore DSPs targeting next-generation-multimedia applications. The company delivers high-perform-



ance, scalable DSP programmable platforms for video and imaging in security and surveillance, high-performance imaging, and broadcast and IPTV (Internet Protocol television) head-end-infrastructure applications. The CT3616, Cradle's flagship multicore system, can provide real-time encoding of Main Profile H.264 at D1 resolution on one chip.

The company's Eclipse-based multicore-development tools support project-management automation and code development in C, C++, and C-like assembly. The development environment includes the Inspector graphical-debugging environment, the graphic runtime-analysis multicore profiling tool, and an extensive library of modules for video, image, and I/O processing.

EVATRONIX
WWW.EVATRONIX.PL

Evatronix offers IP (intellectual-property) cores and electronic-design services, including a range of processor, USB, serial-interface-controller, data-communication, and networking cores. It also offers two families of programmable-DSP cores. The 16-bit C32025 family targets industrial, home, and consumer applications, and the 24-bit C56000 core targets more complex and accurate applications, such as audio compression and image processing.

FREESCALE SEMICONDUCTOR
WWW.FREESCALE.COM

Freescale Semiconductor designs and manufactures embedded semiconductors for the automotive, consumer, industrial, and networking markets. Freescale offers programmable DSPs based on StarCore technology that target advanced communications and networking-infrastructure equipment. The company also offers advanced 16-bit DSCs (digital-signal controllers) for factory automation, building/lighting control, and a range of motor-control applications, such as large appliances.

Last year, Freescale introduced the MSC8156 DSP, a six-core device based on new SC3850 StarCore DSP core technology, to advance the capabilities of wireless-broadband-base-station equipment. Freescale bases the MSC8156 on 45-nm-process technology. The company designed the high-performance multicore DSP to deliver the flexibility, integration, and affordability for mainstream, near-term deployment of networks based on LTE (long-term-evolution) technology and other next-generation wireless standards.

HYPERSTONE
WWW.HYPERSTONE.COM

Hyperstone's processors provide integrated RISC/DSP functions for applications requiring a high-speed microprocessor with a high-performance DSP. These processors feature dual execution units in a pipelined architecture sharing the same registers. The system can mix RISC- and DSP-specific programming transparently to the programmer. RISC/DSP instructions execute with a high degree of parallelism, resulting in high throughput. Typical applications include telephony, VOIP (voice-over-Internet Protocol) telephony, video, digital cameras, general signal processing, and more.

Hyperstone builds its HyNet series of networking processors with its RISC/DSP core and adds integrated peripherals supporting high-speed communications—including Ethernet, Real-Time Ethernet, serial, and ATM (asynchronous-transfer mode)—additional internal RAM, video interfacing, PCI (peripheral-component-interconnect) support, DMA, and more. These processors target applications requiring high-speed signal processing, communications, or both, including Real-Time Ethernet.

IMPROV SYSTEMS
WWW.IMPROVSYS.COM

Improv Systems offers the configurable, multiprocessor Jazz PSA (programmable-system-architecture) platform, which allows designers to create their own application-based optimized processor cores. Improv's Jazz Processor VLIW (very-long-instruction-word) architecture employs parallel execution of operations, targeting computationally intensive applications, such as media processing, digital-signal processing, and communication applications. The general-purpose, fixed-point Jazz DSP cores target general DSP programming.

The Jazz PSA standard tool suite includes the Jazz PSA compiler for VLIW and DSP optimization. The Jazz PSA standard tool suite is retargetable to any configuration of the Jazz PSA platform. The Jazz PSA composer tool suite is an associated graphical-user-interface environment for creating designer-defined DSP cores.

Jazz Media cores include video-, audio-, image-, and speech-processing implementations targeting consumer-electronics devices ranging from mobile handsets and portable media players to high-definition digital displays. Jazz Voice cores address the needs of the voice-over-packet market, including all points of the voice network.

INFINEON TECHNOLOGIES
WWW.INFINEON.COM

Infineon Technologies offers 8-, 16-, and 32-bit DSC (digital-signal-controller) and microcontroller families with DSP capabilities. The 8-bit XC800 family incorporates a Vector Computer unit for sensorless vector control or field-oriented control applications. The 16-bit XE16x DSC family, with integrated MAC (multiply/accumulate) and PWM (pulse-width-modulation) units, targets such motor-control schemes as constant-VF, frequency slip, and field-oriented control. The 32-bit TC116X family, which Infineon bases on the TriCore unified-microcomputer/DSP architecture, targets applications such as servo control, audio-domain digital-signal processing, data communications, modems, automotive systems, and portable systems.

In 2008, Infineon expanded its DSC family with the XE164/167 devices, featuring a MAC unit for dedicated filtering algorithms, and the XE16xM family for safety applications with an added memory-protection unit, memory checkers, and error correction for flash and SRAMs. In 8-bit devices, the XC878 offers as much as 64 kbytes of flash and two independent PWMs to handle vector control plus PFC (power-factor-correction) circuitry, enabling power-efficient single- or dual-motor-control applications from a single chip. Both the 8- and the 16-bit lines saw the release of development kits for BLDC (brushless-dc)- and stepper-motor-control applications, including software-generation tools for various types of motors or control algorithms. In 32 bits, the new TC1700 series extends the TriCore family of single-chip microcontroller/DSP devices.

LATTICE SEMICONDUCTOR
WWW.LATTICESEMI.COM

Lattice Semiconductor provides FPGAs, CPLDs, and programmable mixed-signal devices. Four of its FPGA families will be of interest to DSP designers. The nonvolatile Lattice XP2 family combines flash configuration memory, LUT (look-up-table) logic, and embedded memory and DSP blocks. You can program the embedded DSP blocks to implement functions such as multiply, MAC (multiply/accumulate), and multiply-add/subtract. The Lattice XP2 devices provide as many as 40,000 LUTs, 32 18×18-bit multipliers, and 885 kbits of embedded memory.

The low-cost Lattice ECP2 and Lattice ECP2M FPGA devices provide as many as 100,000 LUTs, 168 18×18-bit multipliers, 5.3 Mbits of block memory, embedded DSP blocks, and 16 channels of 3.125-Gbps SERDES (serializer/deserializer).

Announced in February 2009, the new 65-nm Lattice ECP3 FPGA family offers low power consumption and price for any SERDES-based FPGA devices. The Lattice ECP3 family offers multiprotocol 3.2G SERDES with XAUI (10-Gbit-attachment-unit-interface) jitter compliance, DDR3-memory interfaces, powerful DSP capabilities, high-density on-chip memory, and as many as 149,000 LUTs.

Lattice provides many IP (intellectual-property) cores, including an FFT (fast-Fourier-transform) compiler, a FIR (finite-impulse-response)-filter generator, Reed-Solomon encoders and decoders, convolution encoders, Viterbi decoders, and turbo-coding functions. Lattice includes all these IP cores in its Lattice IPexpress tool, which allows users to parameterize and generate IP on their desktops. It also provides The MathWorks' Matlab/Simulink block set. Lattice includes the IPexpress tool and Simulink block in its comprehensive ispLever 7.2 design-tool suite, which it introduced in December 2008.

MICROCHIP TECHNOLOGY
WWW.MICROCHIP.COM/DSPIC

Microchip's dsPIC DSC (digital-signal controller) is a 16-bit-data modified-Harvard RISC machine that combines the control advantages of a high-performance 16-bit microcontroller with the high computation speed of a fully implemented DSP to produce a tightly coupled, single-chip, single-instruction-stream option for embedded-system design. All of Microchip's 16-bit DSC and microcontroller families share the same DSC- and DSP-core instructions, peripherals, development tools, and pinouts.

During the year, Microchip released to production 26 dsPIC DSCs in the 40-MIPS dsPIC33F family, delivering peripherals and performance for motor control, power supplies, and general-purpose embedded-system applications. The cumulative total of dsPIC DSCs in production now stands at 81. These new products include 13 dsPIC33 general-purpose-family DSCs and 13 dsPIC33 motor-control- and power-conversion-family DSCs. They offer as much as 128 kbytes of flash memory in packages as small as 6×6 mm. Selected DSCs include a new 16-bit peripheral for Microchip—a dual-channel, 16-bit audio DAC. Some DSCs also offer an on-chip CAN (controller-area-network) 2.0B module, a codec interface supporting the I²S (inter-IC-sound) and AC97 (audio-codec-97) protocols, and a parallel master port to communicate with a variety of parallel devices, such as communications peripherals, LCDs, external memory devices, and microcontrollers. Some motor-control members offer a second quadrature-encoder interface, also a first for Microchip's DSCs. The dsPIC33F family continues to grow, with flash memory ranging from 12 to 256 kbytes and pin counts of 18 to 100 pins in a number of peripheral configurations.

New DSC-development tools include the MPlab starter kit for dsPIC DSCs, which aids in adding digital audio to embedded designs. For $59.98, the kit provides a complete development system, including debugger, programmer, IDE (integrated development environment), and C compiler. Also, a new low-cost motor-control board supports dsPIC33F-based, low-voltage BLDC (brushless-dc) designs—the dsPICDEMTM MCLV development board. For $150, the board provides the power-electronics stage necessary to drive motors with no additional hardware.

MIPS TECHNOLOGIES
WWW.MIPS.COM

MIPS Technologies offers a line of processor cores for DTV, broadband access, Wi-Fi, cable set-top boxes, DVD recorders, HD DVDs, and VOIP (voice-over-Internet Protocol) applications. The fully-synthesizable, 32-bit MIPS32 74K cores can achieve operating frequencies greater than 1 GHz in 65 nm. The MIPS DSP ASE (application-specific extensions) Revision 2 includes 74 built-in DSP instructions that can eliminate the need for a separate DSP core. Four 64-bit accumulator registers that provide fast local storage boost signal-processing performance. A robust suite of software-development tools, the MIPS DSP Library, and a third-party DSP applications network support the 74K core family.

NXP SEMICONDUCTORS
WWW.NXP.COM

NXP creates semiconductors, systems, and software that deliver better sensory experiences in TVs, set-top boxes, identification applications, mobile phones, cars, and a range of other electronic devices. In those fields, NXP leverages a long history and active R&D investment in DSP technology.

Based on the TriMedia DSP technology, the PNX1005, PNX1002, PNX1700, and PNX1500 media-processor series target video and complex audio processing, in security and surveillance and videoconferencing and professional-videoapplications. NXP has optimized its latest video DSP, the PNX1005, for h264 video codec, intelligent video analysis, and video enhancement. The company also offers the PNX1002 dedicated audio processor for 16-channel audio acoustic processing. Special versions for the automotive and industrial market are also available.

The CoolFlux DSP is an ultralow-power programmable core for portable-audio applications. It targets headsets, hearing devices, and portable audio players. This C-language-friendly audio-DSP core combines low gate count with high performance. NXP uses the CoolFlux DSP for custom-designed chips, and the DSP is part of a global technology-licensing program, resulting in a well-supported DSP platform and ecosystem.

Building upon the success of the CoolFlux DSP, NXP created a new embedded DSP core for ultralow-power software-defined digital-radio baseband processing and sensor processing. This CoolFlux BSP (baseband-signal processor) extends the classic CoolFlux DSP core with complex arithmetic, SIMD (single-instruction/multiple-data) parallelism and Viterbi and FFT (fast-Fourier-transform) instructions.

OCTASIC
WWW.OCTASIC.COM

Octasic is a global provider of DSP silicon and software products for the converged-carrier-, enterprise-, and endpoint-communication-equipment markets. The company bases its DSP products on the Opus asynchronous-DSP architecture. Octasic's Vocallo multicore media-gateway DSP product, the first Octasic product the company based on the Opus core, represents a new generation of multicore DSPs for media gateways.

Throughout 2008, Octasic expanded its international presence with the hiring of new sales representatives for North America, Korea, and China, and announced EuroSemi GmBH as the company's official representative in Europe. The company built on the Vocallo media-gateway platform for voice by adding video capabilities to create a true off-the-shelf media-gateway product.

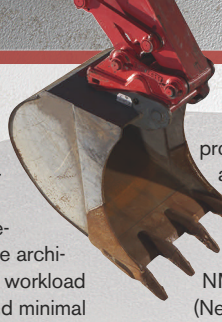
ON DEMAND MICROELECTRONICS
WWW.ODM.AT

ODM (On Demand Microelectronics) offers IP (intellectual property) and SOCs (systems on chips) targeting the upcoming global digital-video revolution. The basis for ODM's product portfolio is the silicon-proven VSP (video-signal processor)—a scalable, configurable, and fully software-programmable processor. The VSP is suitable for handling DSP applications with extremely high-performance demands, such as digital video. The SVEN (scalable video engine) IP core can handle high-definition, multistandard-compliant video-codec implementations for resolutions reaching 1080i/720p. Supporting SVEN, ODM offers the Pictor image-processing platform for high-end image processing, and Samba, the first IP for multistandard baseband processing.

NEW ON SEMICONDUCTOR
WWW.ONSEMI.COM

ON Semiconductor supplies power- and signal-management products. The company's BelaSigna product line of ultralow-power audio-processing systems targets portable-system applications, such as mobile handsets and accessories, hands-free communication, industrial hearing protection, and ALDs (assistive-listening devices).

Innovations over the past year include the BelaSigna 300, an ultralow-power, high-fidelity audio processor for portable communication devices that delivers audio clarity without compromising size or battery life. With 24-bit precision computing, the BelaSigna 300



eliminates noise and echo from communications channels and still has resources for additional audio-management features. The dual-core architecture ensures a balanced workload for processing efficiency and minimal power consumption. Because it is a small audio-processing system, you can design the BelaSigna 300 WLCSP (wafer-level chip-scale packaging) package into PCB (printed-circuit-board) layouts with little or no impact on the size of the end product.

PICOCHIP
WWW.PICOCHIP.COM

PicoChip's family of high-performance multicore-DSP processors includes 200 to 300 processors, each a 16-bit Harvard architecture that is programmable with ANSI C, to deliver total performance of 200 GIPS/30 GMACS. Although these processors are usable for any high-performance-DSP application, the company primarily focuses on the wireless infrastructure. The processor finds use in base stations as a common platform for both WiMax and LTE (long-term evolution). It also supports baseband for femtocells, small base stations for indoor coverage. The company released several new reference designs, including support for WiMax Wave 2 with MIMO (multiple input/multiple output), a WiMax femtocell access point, and a TD-SCDMA (time-division-synchronous-code-division multiple-access) femtocell.

PIXELWORKS
WWW.PIXELWORKS.COM

Pixelworks designs, develops, and markets semiconductors and software for the advanced-display industry, including advanced televisions, multimedia projectors, digital-streaming-media devices, and LCD panels. Pixelworks' line of programmable BSPs (broadband-signal processors) can handle multiple codecs for high-quality IPTV (Internet Protocol television) video and other digital-video applications. The company offers the DreamStream application-reference software for designers using the BSP chips. In addition to the BSP ICs, Pixelworks offers devices ranging from single-purpose discrete ICs to SOCs (systems on chips) that can process and enhance the video signal throughout the entire path in the system.

RC MODULE
WWW.MODULE.RU

The RC (Research Center) Module design center provides IP (intellectual property) for VLIW/SIMD (very-long-instruction-word/single-instruction/multiple-data) processors with a flexible and high-performance vector-matrix engine. The architecture targets industrial video-image processing and navigation and provides scalable performance by employing a programmable operand width of 1 to 64 bits. This flexibility allows designers to trade precision for performance. The NeuroMatrix DSP family includes NM64xx chips and synthesizable NMC (NeuroMatrix core).

The new NMC3 is the next generation of the NeuroMatrix-core family with performance that offers an eight-stage pipeline and 8000-instruction cache that supports eight read/write memory operations per clock cycle and accelerated vector unit operand loads. RC Module offers a SOC (system-on-chip) design service that it bases on NMC3 and ARM's ARM1176JZF-S core. Software- and hardware-development tools, as well as real-time signal- and video-image-processing systems, are available from RC Module.

RENESAS TECHNOLOGY
WWW.RENESAS.COM

For applications that require DSP capabilities, Renesas offers devices with a built-in FPU (floating-point unit). Among them are the SuperH devices in the SH-2A and SH-4A series of high-performance, 32-bit RISC processors. By combining both DSP and FPU capabilities into a single RISC CPU core, they save power and overall system cost.

Recent introductions in the SH-2A series include the SH7262 and SH7264, which offer an FPU and 1 Mbyte of on-chip SRAM for digital-audio systems and graphical-display applications. The new SH-4AL-DSP-based SH7366 processor provides multimedia support, including a VPU (video-processing unit) and USB. For portable multimedia systems, the 400-MHz SH7723 delivers 2.8-GFLOPS performance and supports a video-processing function, a 2-D graphics accelerator, and USB. A new audio-video-player media-reference platform employs Renesas' SH7263 microcontroller, and Express Logic's ThreadX RTOS supports it.

Renesas' 90-nm-based SH74504 and SH74513 devices provide the performance and memory to target advanced driver-assistance safety systems. The 600-MHz SH77650 SOC (system on chip) targets in-vehicle image-recognition-processing applications, and the SH77721 SOC is suitable for low-range to midrange car-navigation systems. With 1920-MIPS performance at 533 MHz, the SH7786 dual-core processor also incorporates a fast DDR3-SDRAM interface for data transfers as fast as 4.27 Gbytes/sec, making it suitable for multimedia systems and next-generation car-navigation systems.

RF ENGINES
WWW.RFENGINES.COM

RFEL (RF Engines) provides high-specification DSP products for FPGAs, as well as digital receivers and products for the defense, government-services, communications, and instrumentation markets around the world. Applications include communications base stations, satellite-communications systems, test-and-measurement instrumentation, and custom wideband receivers/transceivers. RFEL's cores and SOC (system-on-chip) designs primarily target Xilinx and Altera FPGAs.

RFEL's FPGA designs are available as firmware, in COTS (commercial-off-the-shelf) or custom hardware, or in finished products. The standard range of cores includes the HyperSpeed cores for applications requiring as much as 6.4G-sample/sec performance. The HyperLength cores provide as many as 1 million-point transforms, typically running at complex sample rates of as many as 200M samples/sec on Xilinx devices. The Matrix range includes sets of different-length DFT (discrete-Fourier-transform) cores, which, when you combine them, allow the configuration of FFTs (fast Fourier transforms) to match the precise number of points for specific applications.

You can use ChannelCore64 for extracting as many as 64 narrowband channels from one or two wideband ADC inputs. RFEL bases the core on a novel channelization architecture that provides the flexibility you traditionally associate with DDC (direct-digital-control) cores and ASIC devices but with greater silicon efficiency. The main features are 64 independent downconversion channels, support for two 16-bit ADC inputs reaching 220M samples/sec, alias-free channel bandwidths, as much as 687.5 kHz, independent tuning of channel center frequencies with a resolution of less than 0.01 Hz, and a fractional resampler for setting output sample rates with a resolution of less than 0.01 Hz. You can reconfigure channels without affecting operation of other channels. The core supports an end-to-end dynamic range of more than 80 dB as well as gain control.

SENSORY
WWW.SENSORYINC.COM

Sensory's RSC family of devices performs recognition, speech synthesis, and general-purpose product control. The RSC line supports speaker-independent recognition, speaker-dependent recognition, speaker verification for voice biometric security, 2400-bps speech compression for speech playback, and music synthesis. The RSC-4x family provides on-chip integration of features, including a microphone preamplifier, twin-DMA units, a vector accelerator, and a hardware multiplier—all of which allow a designer to build a system with little more than a battery, a speaker, a microphone, and a few resistors and capacitors. Multiple ROM options are available. Sensory's SC-6x series of DSPs offer multiple options for introducing speech-

and music-synthesis abilities into consumer products. Members of the SC-6x line can store as much as 37 minutes of speech on-chip and include as many as 64 I/O pins for external interfacing.

SILICON HIVE
WWW.SILICONHIVE.COM

Silicon Hive, a supplier of semiconductor IP (intellectual property), designs, builds, and licenses application-specific products for communications and media processing; tuned processor cores; and program-development tools with application libraries. Silicon Hive-processor cores target the requirements of an application domain and are high-level-programmable from ANSI C.

The company's processor lineup includes the Avispa-CH1, a high-performance C-programmable data processor for communications-signal processing. The Avispa-IM2 is a general-purpose C-programmable data processor. These two processors are scalable to a high level of operations per cycle, with multiple options for precision, I/O, and memory configurations. The Moustique-IC2 is a C-programmable SIMD (single-instruction/multiple-data) processor targeting image-signal-processing applications with multiple options for SIMD-vector dimension, I/O, and memory configurations. All processors come with a software-development environment, application libraries, and preproven SOC (system-on-chip) integration and verification packages.

SOUND DESIGN TECHNOLOGIES
WWW.SOUNDDESIGN TECHNOLOGIES.COM

Sound Design Technologies provides ultralow-power-DSP products for audio processing, and the company offers 3-D MCM (multichip-module), SIP (system-in-package), and HDI (high-density-interconnect) substrate technologies. The Voyageur programmable multiprocessor-DSP platform maximizes instructions per microwatt using a reconfigurable architecture and an integrated high-resolution ADC and DAC in a miniaturized package. The reconfigurable multicore system consists of hardware accelerators and DSP cores. The system comprises five embedded DSP cores, four of which contain dual MACs (multiply/accumulate) units with a customized instruction set for audio processing, including single-cycle log and exponent functions. Hardware accelerators include FFT/IFFT (fast-Fourier-transform/inverse-FFT) accelerators, hard-wired FENG (filter-engine blocks) of FIR (finite-impulse-response) and IIR (infinite-impulse-response) filters, and a perfect-reconstruction-programmable time-domain filter bank for sub-band audio processing.

GUIDE (Gennum universal integrated development environment), the Voyageur platform-development tool, supports developers' efforts for firmware development, debugging, and testing.

STMICROELECTRONICS
WWW.STM.COM

STMicroelectronics' portfolio includes application-specific products containing a large amount of proprietary IP (intellectual-property) content and multisegment products that range from discrete devices to high-performance microcontrollers, secure smart-card chips, and MEMS (microelectromechanical-systems) devices. Within its portfolio of products, ST develops a family of high-performance VLIW (very-long-instruction-word) cores primarily targeting the consumer, mobile, and computer and peripherals markets.

STREAM PROCESSORS
WWW.STREAMPROCESSORS.COM

Fabless semiconductor company SPI (Stream Processors Inc) offers parallel-processor options targeting consumer and industrial applications. Its Stream-processor architecture brings down computing cost to ASIC levels and makes the performance benefits of parallel processing easily accessible to programmers. Delivering more than 200 GMACS, SPI's C-programmable Stream processors enable designers to adopt a software-driven model and eliminate dependencies on inflexible ASICs or complex multi-DSP or FPGA implementations.

The company's Storm-1 family supports video- and image-processing applications, such as intelligent video surveillance, high-definition videoconferencing, broadcasting, and multifunction printers. The Storm-1 family comprises four software-compatible products—from the low-cost, low-power SP8LP-G30, suitable as a single-chip IP (Internet Protocol) camera product, to the SP16HP-G220, which delivers 448 GOPS of computing performance and targets high-end-imaging and multichannel-video applications. Available RapiDev Tools Suite, development kits, libraries, and a network of third-party developers help customers shorten time to market and slash total costs.

The Stream-processor architecture combines data parallelism with a sophisticated C-development environment to simplify the programming task. To the programmer, the processor looks like a single core, in which the tools and underlying hardware manage synchronization, on-chip memory, and data movement. The compiler-managed memory hierarchy provides predictable performance, high ALU (arithmetic-logic-unit) use, and efficient bandwidth management.

STRETCH
WWW.STRETCHINC.COM

Stretch offers a family of software-configu-

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rable processors with embedded programmable logic within the processor to target imaging and video, mobile/wireless, security, and industrial applications. Using C/C++ programming tools, system developers can automatically configure Stretch's processors to address changing application needs. Stretch's S6000 family of software-configurable processors targets high-performance video and wireless signal processing. The S6 Architecture offers a second-generation ISEF (instruction-set-extension fabric), a processor array, and a programmable accelerator.

Stretch and its partners offer reference-hardware and software applications for main-profile standard- and high-definition MPEG 2 and H.264 video encoding. Many of the core modules from these applications are available in source code as extension instructions. Stretch and its partners also offer hardware and software applications for WiMax base-station equipment. A number of the physical-layer modules, including FFTs (fast Fourier transforms), forward-error-correction functions, and CRC (cyclic-redundancy checking), are available in source code as extension instructions.

TENSILICA
WWW.TENSILICA.COM

Tensilica offers 32-bit customizable data-plane processors, DSPs, and standard processor cores. The Diamond Standard 108Mini, 212GP, and 232L integrate a 32×32-bit multiplier and 32-bit integer divider. The Diamond Standard 570T includes dual 32×32-bit SIMD (single-instruction/multiple-data) multipliers and a 32-bit integer divider as well as 16-bit DSP instructions. Tensilica's 545CK DSP is a three-issue VLIW (very-long-instruction-word) DSP with eight-way SIMD units, dual 128-bit load/stores, and a Viterbi convolutional coder accelerator.

Tensilica also offers preconfigured DSPs for audio and video. The 330HiFi audio DSP includes dedicated audio instructions to decrease frequency requirements and supports popular audio codecs. The 388VDO video DSP targets D1 (standard-definition) resolution and offers H.264 baseline- and main-profile decoding, H.264 baseline-profile encoding, and other software for JPEG, MPEG, and VC-1/WMV (Windows media video) 9.

Designers can customize Tensilica's Xtensa processors for DSP tasks by configuring predefined elements of the architecture and by inventing new instructions and hardware-execution units for maximum performance. The Xtensa LX2 processor core with the Vectra DSP engine supports wide datapaths and traditional DSP tasks. The Xtensa LX2 can deliver RTL-equivalent I/O through direct interfaces that bypass the local/store operation. The Vectra DSP engine uses 64-bit instruction words containing three-issue slots for ALU (arithmetic-logic-unit), MAC (multiply/accumulate), and load/store operations.

TEXAS INSTRUMENTS
WWW.TI.COM

Texas Instruments offers a broad portfolio of programmable DSPs. The TMS320C5000 DSP platform offers power consumption as low as 0.33 mA/MHz and performance to 600 MIPS for portable media and communication products, including digital-music players, GPS (global-positioning-system) receivers, and portable medical equipments.

TI bases the OMAP (open-multimedia-applications processor) 35x, including OMAP3503, OMAP3515, OMAP3525, and OMAP3530, on the ARM Cortex-A8 core, providing laptop-like performance at handheld-power levels in one chip. The OMAP35x targets portable navigation devices, Internet appliances, and portable patient-monitoring devices. The low-power OMAP-L137 targets industrial, medical, audio, and emerging applications, and TI bases it on an ARM926EJ-S and a C674x DSP core. Developers can leverage the floating-point DSP for real-time, processing-intensive computations, and the on-chip ARM enables graphical user interfaces, touchscreens, networking stacks, and implementation of various high-level operating systems, such as VxWorks, WinCE, and Linux.

The TMS320C6000 DSP platform comprises high-performance fixed- and floating-point DSPs targeting video, imaging, infrastructure, and performance-audio applications. The C6745 and C6747 DSPs merge the precision and ease-of-use advantages of floating point with a combination of connectivity peripherals, low power, and low cost. Targeting industrial, medical, audio, and emerging applications, the devices operate as fast as 300 MHz and consume 62 mW in standby mode and 470 mW in active-power mode. The C6474 high-performance processor integrates three of TI's TMS320C64x+ cores running at 1 GHz each on a single die, delivering 3 GHz of raw DSP performance that consumes one-third less power at two-thirds less DSP cost than discrete processing products. The C6474 provides significant system integration for customers currently using DSP farms for telecommunications, medical-imaging, military-communications, and industrial-vision-inspection end equipment and markets.

Digital-media processors employing TI's DaVinci technology include processors, software, tools, and support for the development of digital-video applications. The DM335, TI's lowest-cost digital-media processor, integrates an ARM926EJ-S core and a video-processing subsystem so that developers can add high-definition video at 720p to their portable-system applications, such as electronic-gaming applications, Internet

radio, e-books, digital telescopes, universal remote controls, and video doorbells. The low-cost, ARM-based TMS320DM357 processor includes a royalty-free H.264 codec at D1 resolution for video compression, as well as MPEG-4, JPEG, and G.711 codecs that require no licensing fees or royalties to TI.

TILERA
WWW.TILERA.COM

Tilera offers high-performance multicore processors targeting embedded-networking, security, multimedia-processing, and wireless-infrastructure applications. The Tile processor family targets applications requiring intensive packet processing for layers 3 through 7 at 1- to 20-Gbps throughput. Services such as deep-packet inspection, flow monitoring, and intrusion prevention are ideal targets for Tilera's processors. In the multimedia and DSP arena, the Tile processors enable HD-video applications, such as videoconferencing, surveillance, and broadcast head-end equipment, as well as wireless backhaul and baseband processing.

The Tile64 processor SOC (system on chip) has 64 full-featured processor cores plus system-integration blocks, including four DDR2-memory controllers with ECC (error-correcting code); two 10-Gbps, four-lane PCIe (peripheral-component-interconnect-express) interfaces; two XAUI (10-Gbit-attachment-unit-interface) 10-GbE (gigabit-Ethernet) controllers; two 1-Gbit RGMII (reduced-gigabit media-independent-interface) Ethernet controllers; and 64 bits of flexible I/O that can support HD-video input or other high-speed interfaces. The device includes 5 Mbytes of cache, and each processor core can independently run a full operating system, such as Linux. It is available in speeds of 600 to 866 MHz.

Tilera based the Tile64 family on a tiled-multicore architecture with a mesh-based on-chip interconnect that delivers as much as 32 Tbps of interconnect bandwidth between the cores and allows scaling the architecture beyond hundreds of cores. In addition to multicore processors, Tilera also offers turnkey PCIe appliance boards and a suite of multicore software-development tools.

Tilera's MDE (multicore-development environment) enables developers to take full advantage of the parallel-processing potential of the Tile-processor architecture. It includes a graphical IDE (integrated development environment) with an ANSI C and C++ compiler, a multicore-aware debugger and profiler, a hardware simulator, and Tilera's powerful iLib parallel-programming library. Tilera also delivers a standard runtime environment using full SMP (symmetric-multiprocessing) Linux 2.6 and a system hypervisor.

VERISILICON
WWW.VERISILICON.COM

VeriSilicon is an IC-design foundry providing custom options and SOC (system-on-chip) turnkey services. The company acquired the ZSP division from LSI. VeriSilicon's licensable ZSP DSP cores and star-IP (intellectual-property)-based SOC (system-on-chip) platforms target application markets for voice and wireless communications and multimedia.

XILINX
WWW.XILINX.COM

Xilinx offers programmable-logic products. Over the last year, the company introduced a high-performance reconfigurable-DSP product and expanded the XtremeDSP development platform to cover low-cost-video development. The Xilinx XtremeDSP development-tools package provides a comprehensive design suite that enables you to use The MathWorks' Matlab and Simulink modeling environments for FPGA design. Use this DSP-design environment early in the design flow to explore hardware options for high-level algorithms or to assemble complete DSP systems for production that include RTL, IP (intellectual property), and embedded processing.

The XtremeDSP tools package includes both a system generator for DSP and the AccelDSP synthesis tool. Together, they form a flexible, integrated, and powerful DSP-development environment for FPGAs. The Xilinx DSP-block set with the system generator helps produce logic for Xilinx programmable devices. More than 90 DSP building blocks are available for the Simulink modeling environment.

XMOS
WWW.XMOS.COM

XMOS is a venture-backed fabless-semiconductor company developing SDS (software-defined silicon)—the next generation of programmable chips. The company's programmable devices are available for $1 to $15. To ensure that development costs do not negate the unit-cost savings, the company offers an innovative way to access the programmable hardware through a software-based design flow that bypasses hardware descriptions and logic synthesis.

XMOS bases its technology on the compact, event-driven, multithreaded XCore processor. This 32-bit RISC processor supports as many as eight threads and integrates support resources in the XCore-tile building block. Multithreading permits concurrent processing of distinct functions, ranging from I/O interfaces to complete software applications. With as much as 400 MIPS per tile, the XCore engine has the performance to implement multiple complex, real-time hardware and software functions.

Intersil Micropower Op Amps

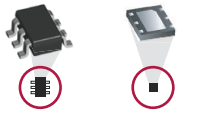
2 < 1

Intersil's pinPOINT™ Precision Analog Product Line now has two single-supply op amps that consume less than 1µA.

Intersil's ISL28194, with a typical supply current of just 330nA, **consumes less than half the power of the closest competitor**. The ISL28195 boasts a gain bandwidth of 10kHz on just 1µA.

Ultra-Small Packages

6 Ld SOT-23 | 6 Ld µTDFN



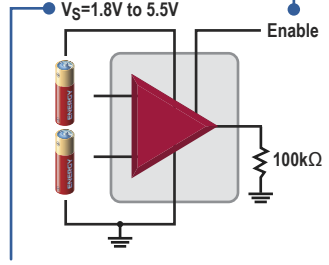
Actual Size (2.6x2.8mm) | Actual Size (1.6x1.6mm)

Other Members of Intersil's Nanopower Family

Device	I_{SS}/Amp (typ)	Function
ISL28194	330nA	Op Amp
ISL28195	1µA	Op Amp
ISL28196	2.5µA	Comparator
ISL28197	800nA	Comparator
ISL60002	400nA	Voltage Reference
X60003	500nA	Voltage Reference

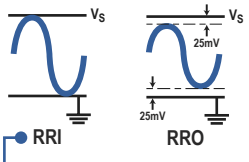
Extended Battery Life:

1. Consumes less current during operation.
2. Consumes only 2nA when amplifier is disabled.



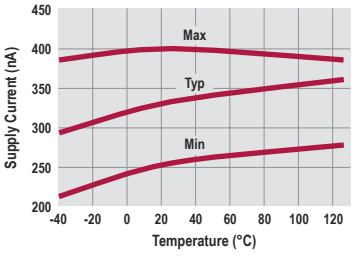
Rail-to-Rail Input/Output

Allows full dynamic range and maximum battery usage.



3. Designed for single-supply operation from 1.8V to 5.5V and ideal for low-power precision applications that run on 1.5V alkaline batteries.
4. True rail-to-rail input simplifes system design and supports maximum signal levels.

ISL28194



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BY DON BRINKMAN • MOLEX

Designing for ROHS: Select the right lead-free-connector design for heat-sensitive applications

THE REMOVAL OF LEAD-BASED ALLOYS, WHICH MANUFACTURERS COMMONLY USE FOR SOLDER AND PLATING, HAS BEEN A MAIN AREA OF CONCERN FOR ENGINEERS DESIGNING ROHS-COMPLIANT ELECTRONICS. LEARN HOW LEAD-FREE ALTERNATIVES AND THEIR ASSOCIATED INCREASE IN REFLOW TEMPERATURES AFFECT CONNECTOR RELIABILITY AND PERFORMANCE.

The ROHS (restriction-of-hazardous-substances) directive, which the EU (European Union) enacted in 2006, aims to prevent environmental damage by restricting the use of lead, mercury, cadmium, hexavalent chromium, PBB (polybrominated biphenyl), and PBDE (polybrominated diphenyl ether). It places greater responsibility on the electronics and manufacturing industries to monitor and regulate the use of these potentially hazardous substances, often components in plastics, base-metal alloys, and the plating and solder processes for electronic-component design.

However, displacement of hazardous substances and compounds, such as those materials ROHS outlines, can affect not only cost and manufacturing time, but also system reliability and performance. As a result, design engineers must be more involved with the manufacturing process to determine the outcome of their end product upon removal of these hazardous materials.

Lead-free alternatives most commonly increase solder-reflow temperatures, heighten MSLs (moisture-sensitivity levels), and reduce elasticity, leading to increases in overall system cost. When selecting lead-free ROHS-compliant components, consider the effect of these changes on various manufacturing processes, such as plated-through-hole and surface-mount technologies.

Lead-free solder commonly requires higher liquidous temperatures—typically, 30 to 35°C more heat than lead-based solder (**Figure 1**). This temperature increase puts some heat-sensitive components at risk during the various soldering processes and can damage components that are not heat-resistant. Therefore, designers should account for all heat-sensitive parts and consult with their manufacturers to identify the necessary assembly-process requirements for lead-free components.

Additional heat can also increase the MSL of the component. Moisture trapped inside the connector can expand and damage the low-profile connectors that slim networking and electronic devices employ. Both solder-temperature levels and the length of time a part is exposed to that temperature can influence a material's MSL. Because the reflow process typically exposes ROHS-compliant materials to more heat compared with leaded materials, they are at greater risk for damage, such as fracturing, joint stress, and delamination due to increased moisture sensitivity.

To prevent any unnecessary absorption of moisture, design engineers must ensure careful handling and packaging of their parts before soldering. Investigating board and part qualifications with the manufacturer before building a product aids in determining which manufacturing conditions are most appropriate for preventing moisture expansion. Some options to consider include baking components before assembly to remove any moisture and packaging the components in humidity-resistant bags.

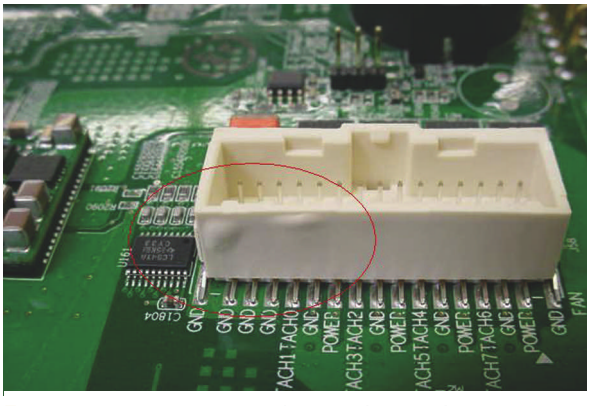


Figure 1 A plastic connector housing blistered after exposure to lead-free soldering temperatures that typically need 30 to 35°C more heat than lead-based solder.

Further, lead-free solders are more rigid and less elastic than those incorporating lead, making them more susceptible to breakage in harsh environments, when under stress, or when exposed to other post-soldering assembly processes, such as hand-soldering or final assembly. As a result, engineers must determine whether to modify a design before incor-

porating lead-free parts. To efficiently account for these factors when designing for ROHS compliance, designers must revisit the manufacturing process behind each product to better qualify which design is most appropriate.

Lead-free plated-through-hole designs use a wave-soldering process to assemble parts to the PCB (printed-circuit board). The technique is primarily for applications in which PCB-space savings is not important. Though the plated-through-hole-mounting style prevents some of the design obstacles associated with the transition to lead-free manufacturing, it does not eliminate all heat-related risks; components can still see exposure to elevated top- and bottom-side preheat temperatures. Studies suggest that wave soldering poses a greater risk of delamination than does oven soldering. *Delamination* refers to the separation of layers within the metal or PCB, causing its internal properties to change. It can be attributable to the repeated stress a PCB goes through as it is exposed to heat, and it affects the reliability of the final product.

Unlike the plated-through-hole process, you create SMT (surface-mount-technology) attachments by treating the board and its components in a reflow soldering oven. As smaller devices and miniaturization become more popular, SMT methods have gained acceptance as a replacement for the through-hole process.

SMT, although suitable for compact designs in cell phones, laptops, and other consumer electronics, increases lead-free components' susceptibility to problems that derive from excess heat. In this process, you screen-print the PCB with solder paste before placing the components on top. Next, the PCB goes through the solder reflow oven, which preheats the PCB and component leads, activates the flux within the solder paste, and reflows the solder paste to create the solder joint between the component leads and the PCB pads. Lead-free SMT parts typically use a tin-, silver-, and copper-solder mixture with a reflow temperature about 34°C greater than lead-based solder. To account for this additional heat, designs that use this mounting method call for high-temperature-resistant plastics, which are generally more expensive than their non-heat-resistant counterparts.

In some niche applications, the solder paste you use for SMT components requires a lower reflow temperature than does the current tin-lead process. In these cases, which use tin-bismuth solder, the liquidous temperature drops to 138°C—well below the 183°C reflow temperature of the tin-lead process—requiring no change in plastic material.

Consult the manufacturer or assembly house at the beginning of the design process to ensure that you are using the correct parts and assembly processes for the design engineer's application and budget requirements.

Unlike SMT components, parts that don't experience any thermal processes need not include high-temperature plastics to survive the manufacturing process. You typically fit compliant-pin, or press-fit, components after all heating steps are complete and lock them into place using friction. Other products in this category include wire-mounted parts, such as crimp terminals, crimp housings, and IDT (insulation-displacement-technology) connectors. These types of temporary mechanical attachments require no solder and rarely encounter heat.

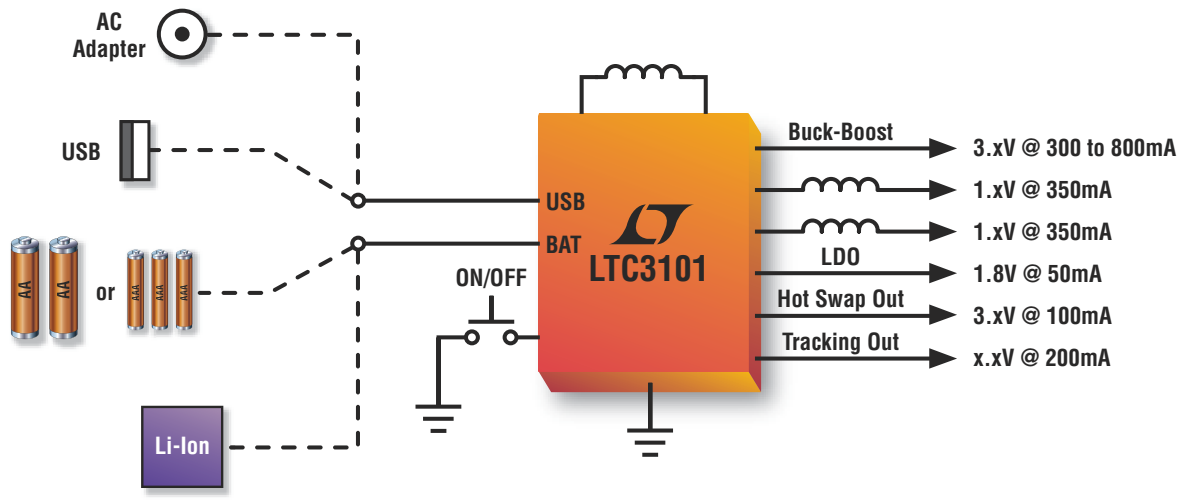
Ideal for high-end-PCB design, these mounting methods help designers avoid problems associated with leadless solder and parts, such as moisture absorption and part malfunction. With an increasing number of initiatives driving the development of "green" design in the electronics industry, accounting for environmental regulations has become a necessary step in the design process.

For heat-sensitive, lead-free components, the displacement of hazardous substances and compounds significantly affects cost and manufacturing, as well as overall system reliability and electronic-component performance. Working closely with manufacturers at the beginning of the design process will help alleviate costs and time. Additionally, studying the methods used to assemble newly ROHS-compliant parts can help you avoid costly adjustments that may not always be necessary. **EDN**

AUTHOR'S BIOGRAPHY

Don Brinkman is manager of engineering information at Molex, where he manages a cross-functional product-development-support group that focuses on engineering systems and processes. He has worked there since 1984 and has participated in the development of nine patents. He received a bachelor's degree in mechanical engineering from the University of Cincinnati (Ohio).

V_{IN} = 1.8V to USB



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Features

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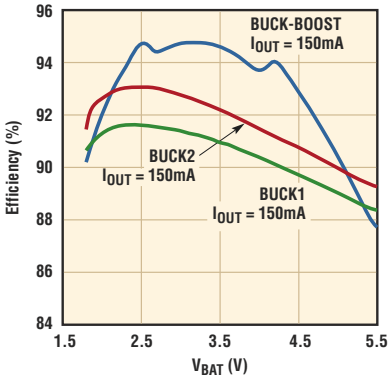
- Buck-Boost Converter with V_{OUT} Range: 1.5V to 5.25V
- Dual 350mA Sync Buck Regulators with V_{OUT} Down to 0.6V
- Pushbutton On/Off Control
- 4mm x 4mm x 0.75mm QFN-24

Efficiency Curve



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designideas
READERS SOLVE DESIGN PROBLEMS

Microcontroller converts digital-temperature-sensor readings without floating-point arithmetic

Jordan Dimitrov, Toronto, ON, Canada

Digital temperature sensors combine a sensor, an ADC, and a serial interface in a single chip. They feature wide enough measurement range, good accuracy and resolution, no need of external parts, easy interface to microcontrollers, small size, and low price. In a review of 10 digital sensors from seven companies, all parts deliver signed-number data in two's-complement format. They feature temperature ranges of −25 to +85 or −40 to +125°C, accuracy of 0.5 to 2 or 2 to 4°C, and output data of 9 to 13 bits with 0.5 to 0.0312°C resolution. The devices' conversion time is 26 to 750 msec, and they use an SPI (serial-peripheral interface), an I²C (inter-integrated-circuit), or a 1-Wire interface. Power supplies are 1.5 to 3.6 or 3 to 5.5V, and prices range from 80 cents to $2.10 (1000).

These sensors connect to microcontrollers; hence, size, speed, and time to develop firmware are also important. The standard approach is to use a high-level language and a compiler. Development time is short, and performing even complex calculations is not a problem. However, compilers produce machine code that occupies more memory and runs at lower speed than code from an assembler. Also, compiler IDEs (integrated development environments) cost hundreds of dollars, whereas many companies offer free assembly-language IDEs. If you work on a tight budget or memory-space allotment, assembly language is the better option. The problem is to find a simple way to avoid the necessary floating-point calculations to convert sensor data into human-understandable format, both in Celsius and Fahrenheit. This Design Idea presents an effective approach.

Consider the TMP121 sensor from Texas Instruments (www.ti.com). It provides 13-bit data in a 16-bit frame with resolution of 0.0625°C/bit. Hence, the transfer function is $t_C=0.0625\times N_S$, where t_C is the temperature in degrees Celsius and N_S is the sensor data after you remove the three meaningless least-significant bits. You can easily rearrange the above **equation** to:

$$t_C=\frac{5}{80}\times N_S=\left(\frac{N_S}{2}+\frac{N_S}{8}\right)\times\frac{1}{10}. \quad (1)$$

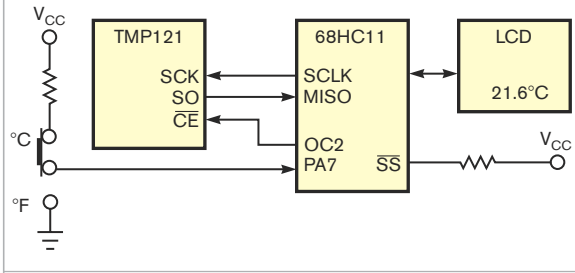

Figure 1 A small system uses a 68HC11 microcontroller to read a switch and a sensor, to convert data, and to display temperature.

DIs Inside

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47 Drive a single-coil latching relay without an H-bridge circuit

48 Limit switches control dc-motor H bridge

50 Implement a clip-detection circuit for BTL Class D amplifiers

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To get readings in degrees Fahrenheit, use the following **equation**, which converts degrees Celsius into degrees Fahrenheit: $t_F=[(9/5)\times t_C+32]$. Replacing t_C from the above **equations** yields:

$$t_F=\frac{9}{5}\times\frac{5}{80}\times N_S+32=\left(N_S+\frac{N_S}{8}+320\right)\times\frac{1}{10}. \quad (2)$$

The benefit of **equations 1** and **2** is that you can perform the calculations with integer arithmetic only. They require divisions by powers of two, which you can replace with shifts, and division by 10, which you perform by introducing a decimal point in the display.

The circuit underwent testing with the popular 68HC11 microcontroller from Motorola (www.motorola.com, **Figure 1**). Besides a sensor and a controller, it includes a unit-selection switch and a dot-matrix LCD. The display resolution is 0.1°. The core of the supporting firmware is an endless loop in which the 68HC11 uses an output-compare function to generate a square-wave signal with a

period of 1 sec and a duty cycle of 50%. The OC2 signal connects to the $\overline{CE}$ input of the sensor and controls its operation: When $\overline{CE}$ is high, the sensor measures temperature. The HC11 does nothing except display M on the LCD. When $\overline{CE}$ becomes low, the last measurement latches in a shift register inside the sensor. The HC11 deletes M from the display, reads the switch and the sensor, manipulates the data, and displays the temperature.

Equations 1 and **2** provide the basis for two source codes. **Listing 1**, available at www.edn.com/090305dia, generates machine code of 981 bytes. **Listing 2**, also available at www.edn.com/090305dia, generates machine code of 392 bytes. Despite the C-language approach with integer arithmetic, it needs 2.5 times more memory to do the job. The ratio is well above 10 if the C code goes with equations that need floating-point arithmetic. The benefit is clear: Modified **equations 1** and **2** and assembly-language programming let you select a microcontroller with less memory and reduce the price of your design. EDN

Discrete-component buck converter drives HB LEDs

Dhananjay V Gadre, Netaji Subhas Institute of Technology, New Delhi, India

HB (high-brightness) LEDs require a large amount of current to operate. When driving HB LEDs from a voltage source, you can set the required current with a suitable series resistor. If the voltage source is a battery, then, as the battery drains, the LED's intensity decreases. Also, a series resistance has the disadvantage of power loss through the resistor. A better option is to use a suitable dc/dc converter. If the LED's turn-on voltage is lower than the battery voltage, as would be the case with a 6V sealed-lead-acid battery, then you can use a buck converter (**references 1** and **2**). You can build a simple buck converter using only discrete components. It requires two bipolar transistors, a P-channel MOSFET, an inductor, a Schottky diode, and a few resistors (**Figure 1**).

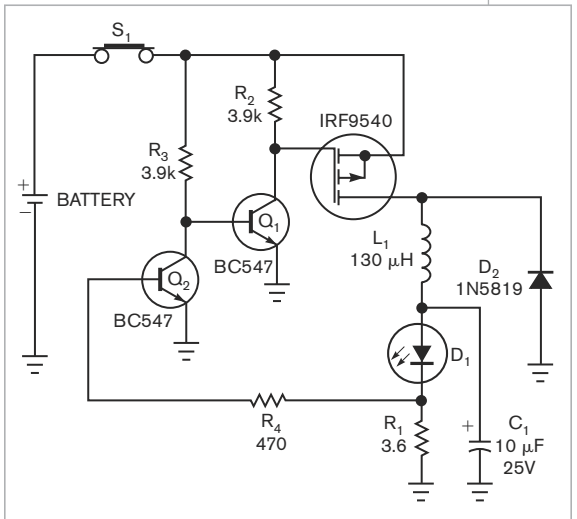

Figure 1 A buck converter provides current sufficient to drive a high-brightness LED.

When you switch on the battery voltage, the voltage across R_1, the resistor in series with the HB LED, is 0V. Thus, transistor Q_2 is off, and Q_1 is in saturation. The saturated state of Q_1 switches on the MOSFET, thereby applying the battery voltage to the LED through the inductor. As the current through resistor R_1 increases, it turns on Q_2, which turns off Q_1 and thus turns off the MOSFET. During the MOSFET's off state, the inductor continues to supply current to the LED through Schottky diode D_2. The HB LED is a 1W, white Lumiled (www.philipslumileds.com) LED. Resistor R_1 helps control the LED's

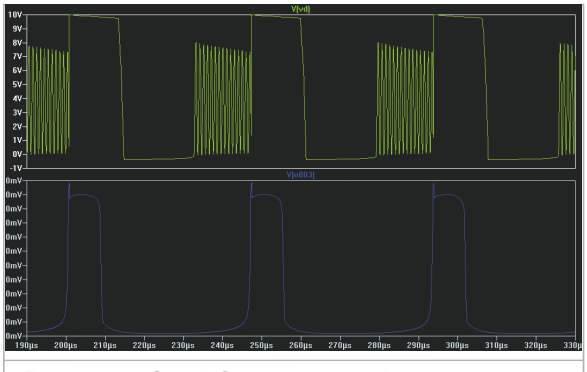

Figure 2 In a SwitchCAD simulation, the upper trace is the MOSFET-drain voltage, and the lower trace is the base voltage of Q_1.

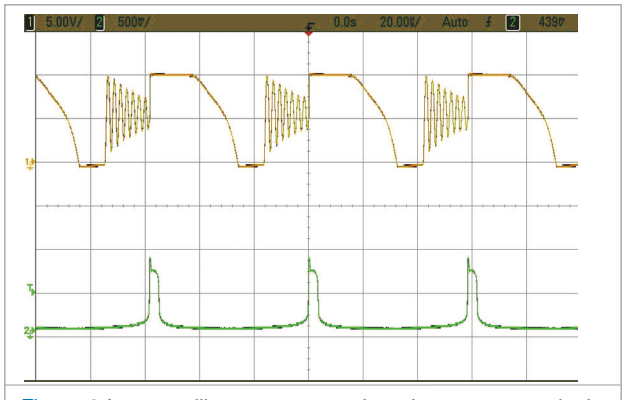

Figure 3 In an oscilloscope screenshot, the upper trace is the MOSFET-drain voltage; the lower trace is Q_1's base voltage.

DESIGN NOTES

Dual Output Buck Regulator with Current Partitioning Optimizes Efficiency in Space-Sensitive Applications

Design Note 460

Johan Strydom

Introduction

The LTC®3546 is a dual output current mode buck regulator with flexible output current partitioning. Beyond the advantages normally associated with dual output regulators (reduced size, cost, EMI and part count, with improved efficiency), the LTC3546's outputs can be partitioned for either 3A and 1A outputs, or two 2A outputs. This increases its application range and simplifies multiple supply rail designs. A configurable Burst Mode® clamp for each output sets the current transition level between Burst Mode operation and forced continuous conduction mode to optimize efficiency over the entire output range. An adjustable switching frequency up to 4MHz and internal power MOSFET switches allow for small and compact footprints.

The LTC3546 utilizes a constant frequency current mode architecture that operates from an input voltage range of 2.25V to 5.5V—well suited to point-of-load (POL) conversion for intermediate power bus applications—and provides dual regulated output voltages as low as 0.6V.

The adjustable switching frequency can be set from 750kHz to 4MHz by an external resistor or synchronized to an external clock, allowing for a significant reduction in overall solution size through the reduction of the output capacitors and inductors. Furthermore, the 180 degree phase shift between outputs reduces input ripple current when compared with two independent regulators, as the ripple frequency is effectively doubled, thereby lowering EMI and allowing the use of a smaller input capacitor while also improving efficiency.

Additional features such as soft-start, supply sequencing and tracking, short-circuit protection and current foldback are all included in a thermally enhanced 28-lead 4mm × 5mm QFN package. An entire converter typically consumes less than 0.6 square inches of board real estate, single-sided, and is limited to 1.2mm in height.

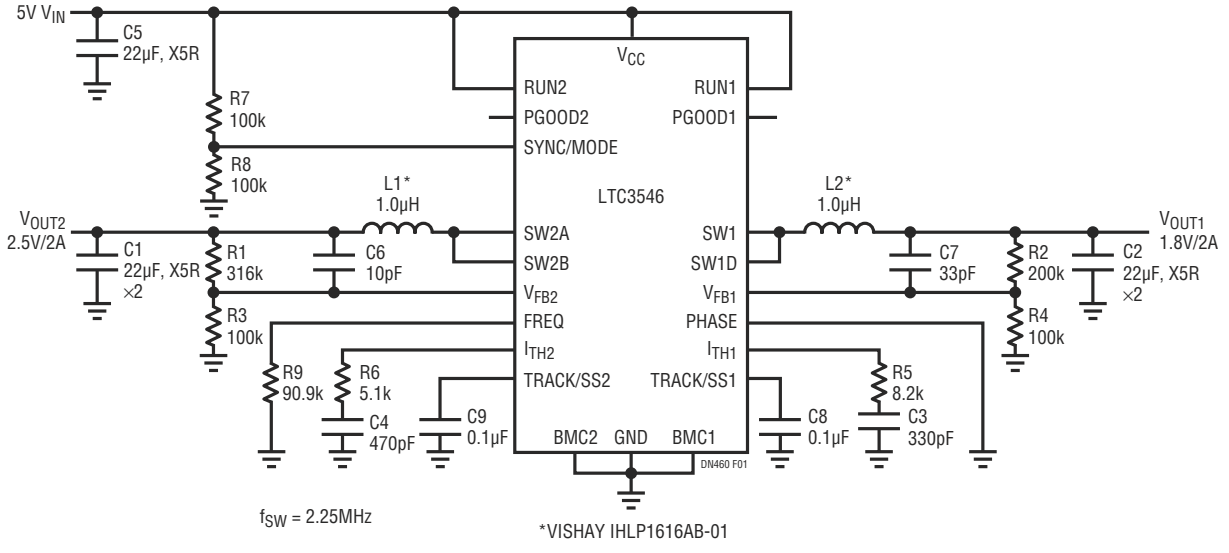

Figure 1. A Low Profile Dual Output Converter for AM Frequency Sensitive Applications—2.5V/2A and 1.8V/2A Outputs

Flexible Current Partitioning

A unique feature of the LTC3546 is its flexible current partitioning. The LTC3546 has two independently regulated outputs that can deliver up to 2A and 1A due to the 90mΩ and 180mΩ internal power MOSFET switches. An additional 1A output, with 180mΩ internal power MOSFET switches, can be paralleled to either of the outputs to produce either a 3A/1A or a 2A/2A dual output regulator. This external connection is internally detected and the dependent output is automatically gated in accordance to the connected output—nothing more is required.

Operation Modes and Efficiency

The LTC3546 can be configured for Burst Mode operation, forced continuous conduction (FCC) operation or pulse-skipping mode. In mobile applications where battery run time is of paramount importance, Burst Mode operation boosts efficiency by reducing gate charge losses at light loads, reducing supply current to just 125µA at no load. When noise control is important, forced continuous conduction operation may be preferred in order to trade efficiency for predictable, easily filtered constant frequency switching regardless of load current. Pulse-skipping mode provides a good compromise between light load efficiency and output voltage ripple. For optimum efficiency over all load conditions, the transition current between Burst Mode operation and forced continuous conduction mode can be set through the Burst Mode clamps (BMC) independently for each output.

Application Examples

Figures 1 and 2 show the versatility of the LTC3546. Figure 1 shows a low profile converter with two independent outputs. It is configured for constant frequency (2.25MHz) operation regardless of load. This design is optimized for space sensitive applications where AM band (520kHz – 1710kHz) interference could be a concern. Figure 2 shows a full featured dual POL converter with Burst Mode operation. The Burst Mode clamps are set for optimum efficiency over the entire load range of each output. This design is best suited for efficiency-sensitive applications with wide load current ranges.

Conclusion

The LTC3546 is a versatile dual output buck regulator suited for low to medium power applications. It delivers all the advantages of a dual output regulator with added flexible load current partitioning. The versatility of the LTC3546 makes it suitable for a wide range of applications that require compact, high efficiency power supplies.

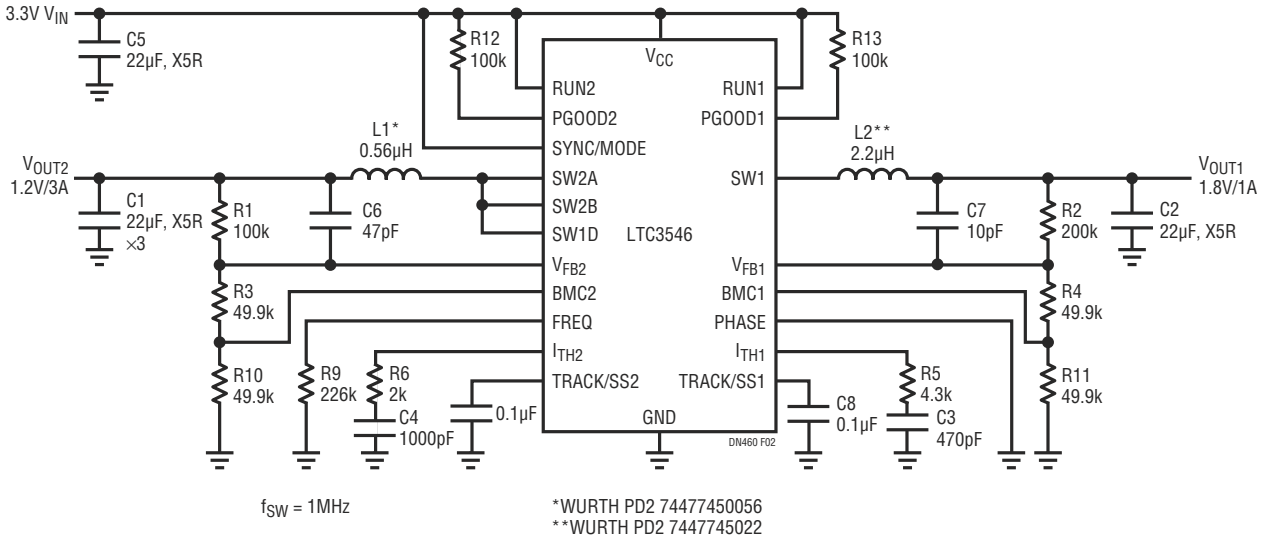

Figure 2. A Dual Output Converter with High Efficiency Over the Entire Output Range—1.8V/1A and 1.2V/3A Outputs

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intensity. Using a larger value for R_1 reduces the intensity.

The SwitchCAD-III software, which is available as a free download from Linear Technology (www.linear.com), simulated the circuit; the simulated MOSFET was an International Rectifier (www.irf.com) IRF9Z24S instead of an IRF9540 because the model for IRF9540 is not available in SwitchCAD-III. **Figure 2** plots the MOSFET-drain waveform and the voltage at Q_1's base. The circuit was wired on a prototyping board and tested for various supply voltages. **Figure 3** shows oscilloscope screenshots for the MOSFET-drain voltage and the voltage at the base of Q_1. They fairly well match the simulated waveform. Conversion efficiencies were 60 to 95% for supply voltages of 6 to 10V. EDN

REFERENCES

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2 Gadre, Dhananjay V, "Buck regulator controls white LED with optical feedback," *EDN*, Oct 25, 2007, pg 72, www.edn.com/article/CA6491146.

Drive a single-coil latching relay without an H-bridge circuit

Carlos Cossio, Santander, Spain

Single-coil latching relays find use in signal-routing, audio, and automotive systems. To maximize their usefulness and cut power consumption, these coil currents must flow in both directions. Current flowing from the latching relay's positive pin to the negative pin causes it to latch in its reset position. Current flowing from the negative pin to the positive pin latches the relay in its set position. The relay maintains its position even when you remove the coil current, which saves power after the relay latches.

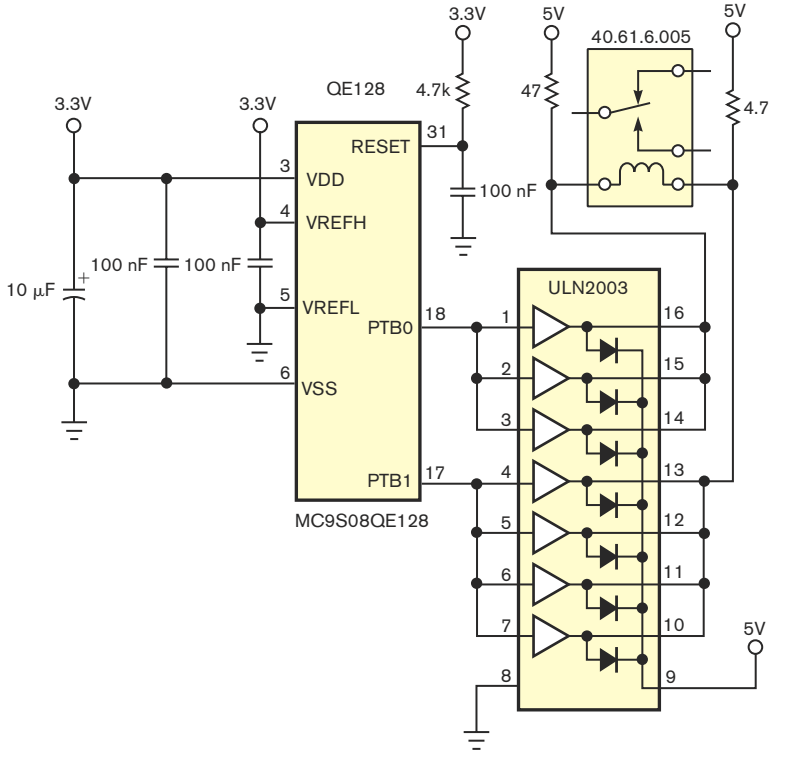

Figure 1 You can drive a single-coil latching relay without an H-bridge circuit, greatly simplifying hardware design and making the most of the low-power-consumption features inherent to latching relays in portable-system applications.

Latching relays have advantages over classic relays because, as soon as the relay switches, it remains in that position without consuming energy. Thus, no current consumption means less heat, smaller heat sinks, and a dramatic increase in battery life for portable devices. In some cases, the use of a latching relay lets your greatly simplify a circuit.

Although latching relays boast significant advantages over classic relays, their use appears limited to niche applications because they require more attention to design details. In general, a latching relay's drive circuit is slightly more complex than that of a classic relay. The traditional approach to driving a latching relay is to use an H-bridge circuit, which can be costly and difficult to handle. In addition, you must design a demagnetization circuit using a special resistor to limit the current in compliance with the manufacturer's specifications.

Figure 1 shows a simple circuit using the MC9S08QE128 microcontroller from Freescale (www.freescale.com) to drive a Finder (www.findernet.com) 40.61.6.005 single-coil latching relay with a standard ULN2003 Darlington driver with open-drain outputs and inductive-kickback protection. Clamping diodes on each ULN2003 output pin catch high-voltage transients that occur when you interrupt the coil current. Because demagnetization uses low-value resistors, you

must wire at least two open-drain buffers of the ULN2003 to both endings of the relay coil to ensure enough current when the microcontroller pulls down.

Listing 1, which is available in the Web version of this Design Idea at www.edn.com/090305dib, shows the software procedure to latch the relay to its set or reset position by turning on the corresponding microcontroller output for at least 50 msec. The current flows into the ULN2003 open-drain output and latches the relay to its set or reset position, according to the direction of the coil current. As soon as the relay latches, drive the corresponding microcontroller output low to turn off the ULN2003 open-drain buffer to ensure the lowest power consumption. You must, however, take into account the set/reset timing. Pull the microcontroller output low only after the required time has elapsed. Waiting ensures that the relay will properly latch to its intended position. EDN

Limit switches control dc-motor H bridge

Andreas Grün, Wedemark, Germany

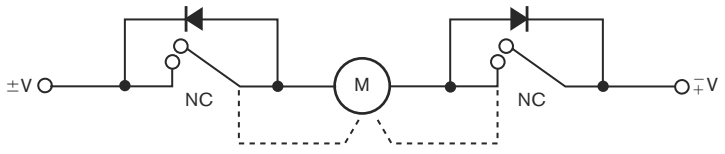

Figure 1 This circuit works by inhibiting movement in one direction but allowing movement in the other direction when the motor retracts from its end position.

You use limit switches to switch off a motor if it reaches one of its two end positions. Even if you build a microprocessor-based motor controller, you should switch off a motor with hardware by building a safety interlock. Such a circuit works by inhibiting movement in one direction but allowing movement in the other direction when the motor retracts from its end position. **Figure 1** shows the circuit with mechanical switches. However, this ancient mechanical approach may be unsuitable in some cases because the motor cur-

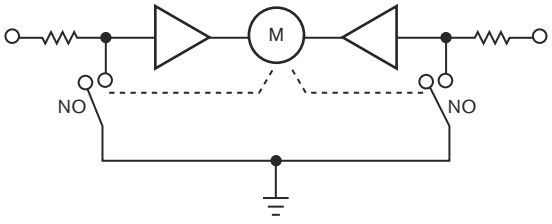

Figure 2 This circuit shortens one input of the H bridge to ground so that movement is possible only in the other direction by turning on the other input.

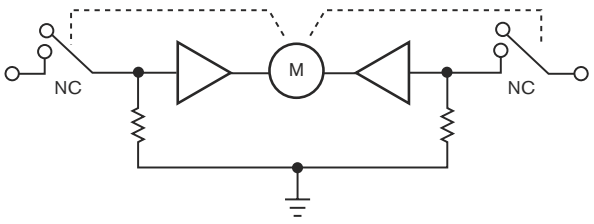

Figure 3 This circuit interrupts the connection to the driving circuit of one input and sets the input to low using a pull-down resistor.

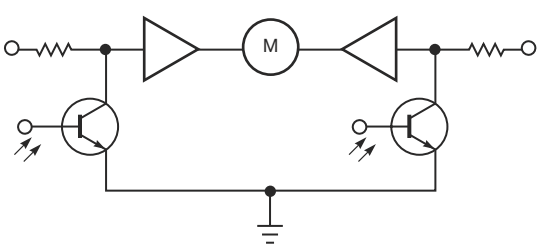

Figure 4 This circuit is the same as that in Figure 3, and it works with phototransistors without modification.

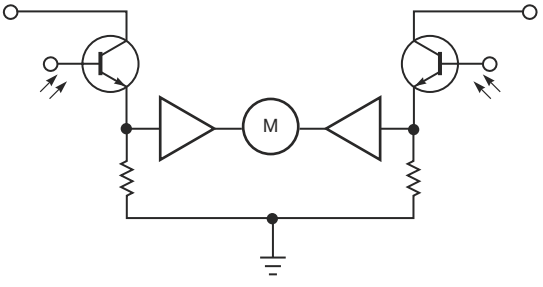

Figure 5 This circuit is the same as that in Figure 4; the value of the resistors depends on the parts you use.

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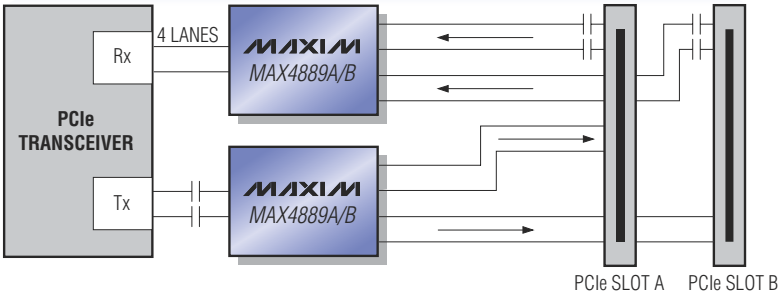

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MAX4889B/C	PCIe 2.0 to 8Gbps	4			
MAX4928A/B	PCIe 1.0 and 2.0, DisplayPort	6		DisplayPort	56-TQFN (5 x 11)

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rent may be too high, or the switches may be closing switches or light barriers.

If you use an H bridge to drive the motor, you can achieve the same operation in a more versatile way. The circuit in **Figure 2** shortens one input of the H bridge to ground so that movement is possible only in the other direction by turning on the other input. If the switches are opening at the end positions, the circuit in **Figure 3** interrupts the connection to the driving circuit of one input and sets the input to low using a pulldown resistor. The same circuit works with phototransistors without modification (**figures 4** and **5**). The value of the resistors depends on the parts you use; a value of 10 kΩ should work in most designs. EDN

Implement a clip-detection circuit for BTL Class D amplifiers

Dimitri Danyuk and Rich Lenser, Niles Audio, Miami, FL

Clip detection is a convenient feature in Class AB amplifiers. It produces a signal from a clip-detection pin that drives an automatic volume control, which reduces gain compression and distortion when the amplifier is overdriven. Class AB amplifiers, such as the STMicroelectronics (www.st.com) TDA7293, TDA7396, STA7360, and STA540 and the Toshiba (www.toshiba.com) TA8275 and TB29xx, have on-chip clip-detection circuits. Newer Class D automotive amplifiers, such as the four-channel STMicroelectronics TDA7454 and the Texas Instruments (www.ti.com) TAS5414/5424, have on-chip clip-detection circuits, but these ICs use a common clip-detection pin, comprising hardware ORed inside the IC, for all four channels. Other Class D amplifiers lack the clip-detection feature altogether, but you can implement it with external components.

An analog-input Class D amplifier comprises PWM (pulse-width-modulation) logic, gate-drive circuits, and a power stage. The PWM logic transforms the analog-input signal into a PWM signal. The power stage with

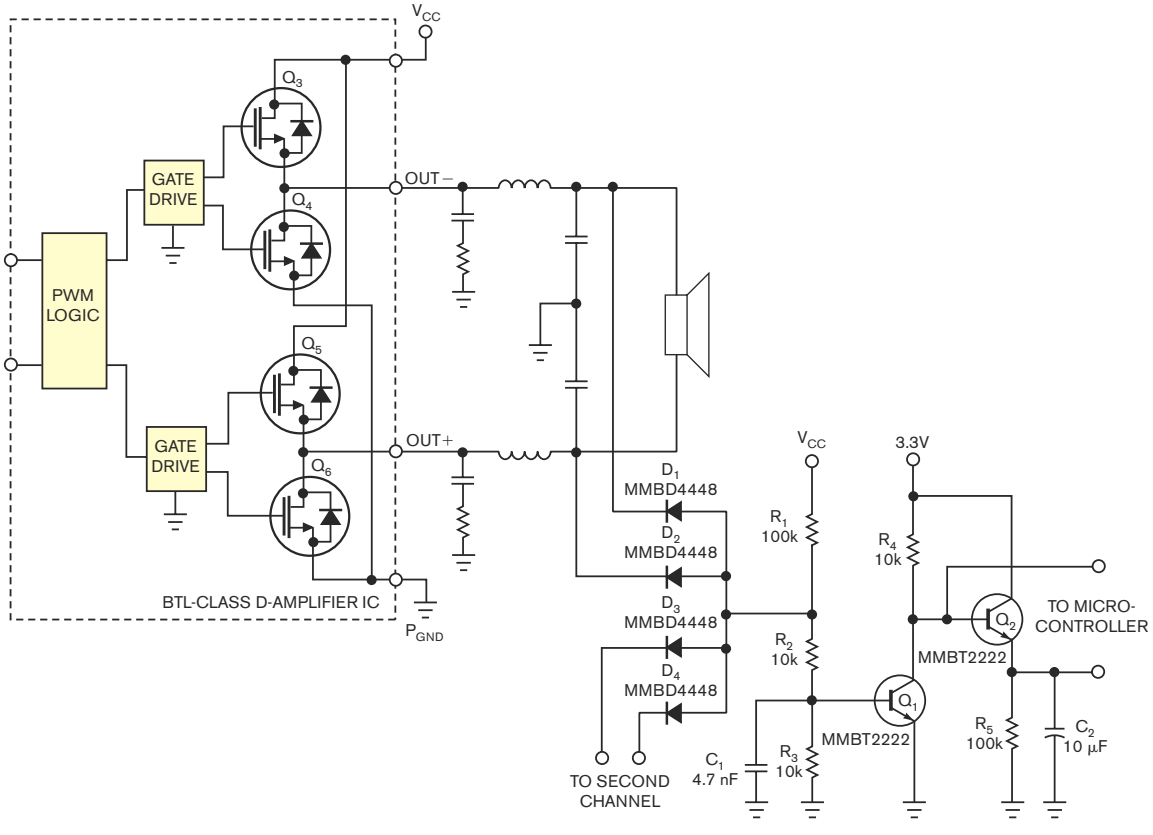

Figure 1 Adding several components to the BTL-Class D-amplifier IC provides a clip-detection function. A peak detector, comprising Q_2, R_5, and C_2, is optional.

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Extensive feature set minimizes external component count

The MAX19517 ADC is a member of Maxim's pin compatible family of ultra-low power, dual-channel ADCs. Its extensive set of features (a partial list is shown below) minimizes external component count and supports a wide range of applications that demand high performance.

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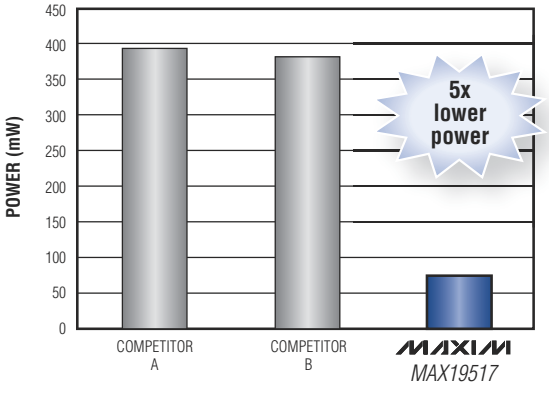
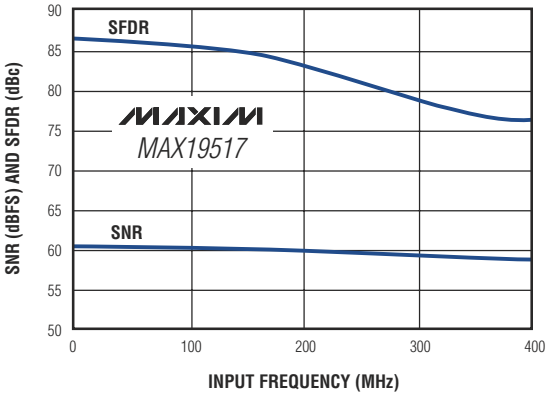


DYNAMIC PERFORMANCE



Selected key features

- Lowest power: 75mW per channel
- Excellent performance for input frequencies from DC to > 400MHz
- Self-sensing supply regulation
- 1.8V, 2.5V, 3.3V operation
- Wide input common-mode range
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- Flexible data formatting
- Programmable data timing
- Programmable clock divider: 1x, 2x, 4x
- Data output test patterns
- 7mm x 7mm, 48-pin TQFN package

Pin-compatible, ultra-low-power, dual-channel ADCs

Part	Resolution (Bits)	Sample Rate (Msps)	Power per Channel (mW)	SNR (dBFS)	SFDR (dBc)
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MAX19516		100	57		
MAX19515		65	43		
MAX19507	8	130	75	49.7	69
MAX19506		100	57		
MAX19505		65	43		

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the gate drivers transforms the low-power PWM signal into a high-voltage, high-current PWM sequence. A BTL (bridge-tied-load) amplifier basically comprises two gate-drive circuits and two power stages, which the same PWM signal drives. The signal directly drives one gate-drive circuit and phase-inverts the other. In theory, a BTL amplifier can produce four times more power into the same load than a single-ended amplifier.

Figure 1 illustrates the implementation of an external clip-detection circuit to a BTL-Class D-amplifier IC. The voltage swing on each output is symmetrical and is within the range of voltage drop on the on-resistance of MOSFET Q_6 to the common-collector voltage, V_{CC}, minus the voltage drop on the on-resistance of MOSFET Q_3. When the output voltage reaches a certain threshold, Q_1 turns off. The component values of R_1, R_2, and R_3 and the voltage drop across diodes D_1 through D_4 set this threshold, which is 0.5V with respect to power ground, P_{GND}, for the given component values. A positive-going pulse appears on the collector of Q_1 whenever the output voltage is below the threshold with respect to power ground. This pulse alerts the host microcontroller to the existence of clipping (**Figure 2**). Capacitor C_1 filters the residual of the switching- and high-frequency content of the audio signal.

A simple application involves filtering and integrating the pulses with further automatic reduction and restoration of the volume setting using the microcontroller's driven-volume control to counteract the clipping distortion. You can also implement more sophisticated algorithms (**Reference 1**). A suitable peak detector comprising Q_2, R_5, and C_2 allows the circuit to hold the short clipping pulses for a longer time. You can add LED circuitry to provide a visual clipping indication. EDN

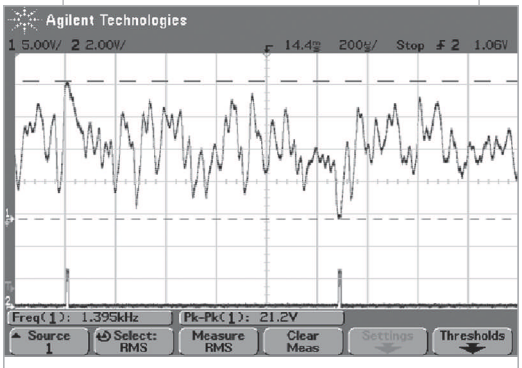

Figure 2 A positive-going pulse appears on the collector of Q_1 whenever the output voltage is below the threshold with respect to power ground.

REFERENCE

1 Person, Andrew P, and James P Muccioli, "Adjustable Clip Detection System," US Patent, 5,453,716, Sept 26, 1995, US Patent Office, http://patft.uspto.gov.

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Distributors' credit practices crucial

If your company is having a tough time getting credit in the current economic environment, it needn't stop investing in design. Despite the global credit crunch, assistance may be no further away than a distributor. Credit practices in the distribution channel haven't changed despite the current economic crisis, according to both distributors and suppliers. "As far as our distributors are concerned, we have not seen any significant changes in … managing credit or in payment terms," says Eric Sussman, director of distribution, Americas, for connector maker Molex Inc (www.molex.com).

Frank Flynn, president of Sager Electronics (www.sager.com), a privately held distributor-based company, agrees: "We haven't experienced any change in behavior within our customer base," he says. "And

we have not modified our behavior in regard to credit." Distributors' willingness to extend credit could become increasingly important to the design community as the economic crisis stretches out. Production orders are the first casualties of a slowdown, as OEMs cut back on manufacturing and distributors worry about inventory. However, design and prototype purchases will be the last to go. OEMs and distributors are less concerned about nonpayment on a $500 order than they are about a $50,000 purchase.

This news is good for companies that are small, design-oriented, or both. For distributors, credit decisions hinge more on a customer's ability to pay than on the overall size of the company.

As risky as the lending environment seems, distributors' willingness to extend credit is good for the supply chain. "Distributors don't manufacture anything, so, if they are managing their inventory levels, they can turn their situation into a cash reserve," Sussman says.

Whatever the economy brings, the electronics industry won't be suffering an inventory glut similar to the one it went through earlier this decade. "We know distributors that have relationships with large OEMs that go for five to 10 years," says Sussman. "It's a good time to place some bets and to lock up business."

–by Barbara Jorgensen

GREEN UPDATE

ECHA OPENS REACH CONSULTATION ON AUTHORIZATION LIST

The ECHA (European Chemicals Agency) has commenced a public consultation on first-draft recommendations to the REACH (registration, evaluation, authorization, and restriction of chemicals) regulation authorization list. The recommendations concern seven substances that the Helsinki, Finland-based ECHA could include on a list of substances subject to authorization under REACH. The substances find use in a variety of electronics as adhesives, sealants, and flame retardants, among other applications.

REACH AUTHORIZATION LIST CANDIDATES

- **musk xylene**
- **short-chain chlorinated paraffins**
- **HBCDD** (hexabromocyclododecane)
- **MDA** (diamino-diphenyl methane)
- **DEHP** (Di [2-ethylhexyl] phthalate)
- **BBP** (benzyl-butyl phthalate)
- **DBP** (dibutyl phthalate)

The first-draft recommendations further propose that manufacturers should submit applications for authorization 24 to 30 months after REACH adds a substance to the authorization list. REACH will prohibit these substances from manufacture, import, or use in manufacturing processes 42 to 48 months after the inclusion date.

ECHA invites interested parties to comment by April 14, 2009, using forms available on the ECHA Web site (www.echa.europa.eu).**–SD**

OUTLOOK

CHINA'S SEMICONDUCTOR MARKET TO FALL

China's semiconductor industry should see a revenue decline in 2009, dropping 5.8% to $72 billion from 2008's $76.5 billion, according to iSuppli Corp (www.isuppli.com).

ISuppli notes that, even during 2001, when global semiconductor revenue plunged 28.6%, China's industry increased 24.4%. But the 5.8% forecast fall is still far below iSuppli's projected 9.4% global semiconductor-revenue decline for 2009, and the company expects China to rebound. ISuppli predicts that growth will return in 2010, with a revenue climb of 9%, followed by an 11% increase in 2011. "China's economy has been increasingly affected by the financial crisis in developed countries since the third quarter of 2008," says Kevin Wang, iSuppli senior manager of China research.

To jump-start the economy, the Chinese government will implement a stimulus package over the next two years and is making major structural changes in its industrial and commercial sectors through new corporate-income-tax and labor laws. Moreover, iSuppli says, the Chinese government will continue to implement more national technical standards, hoping to shield Chinese companies from their more established international competitors.**–SD**

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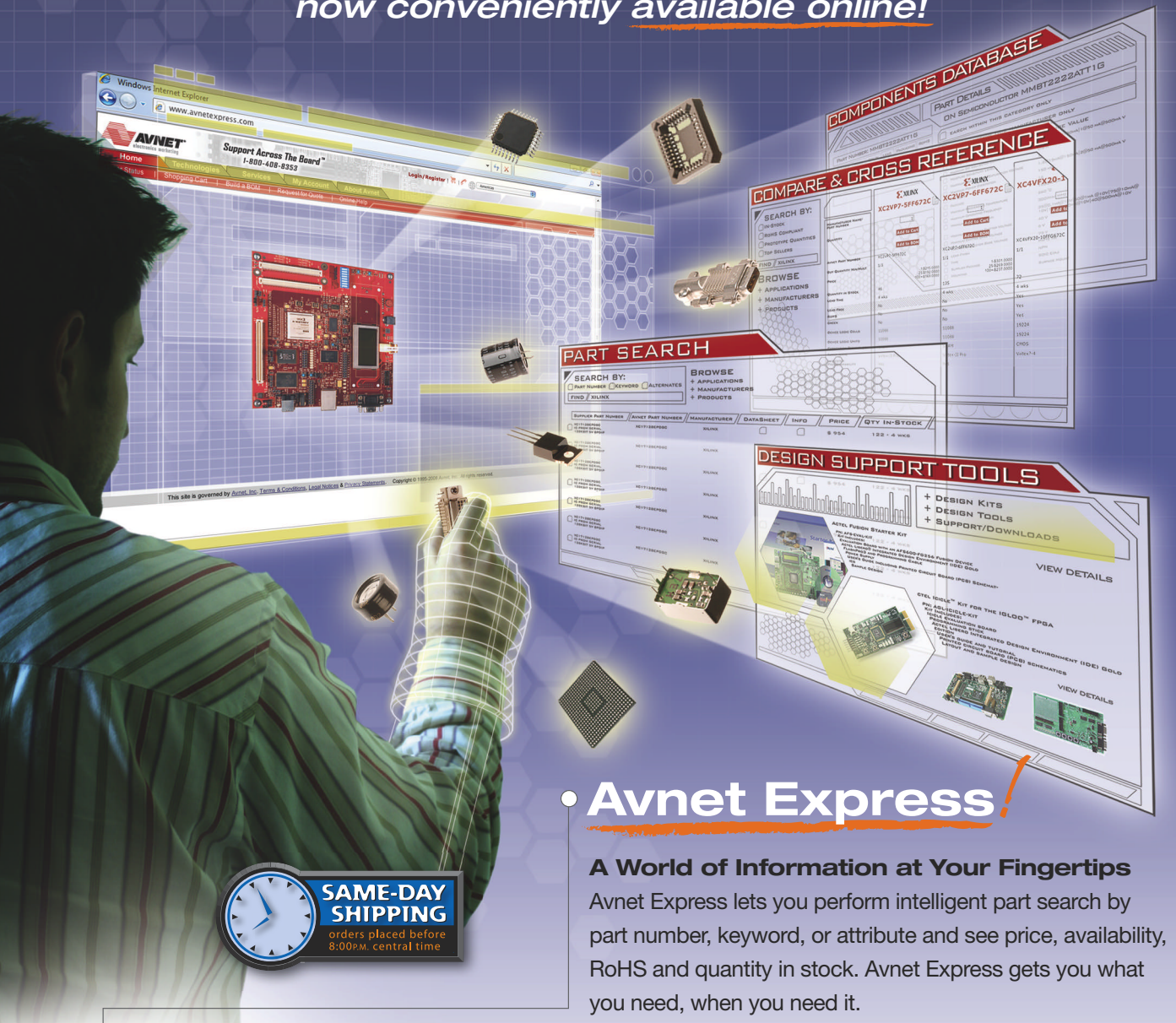

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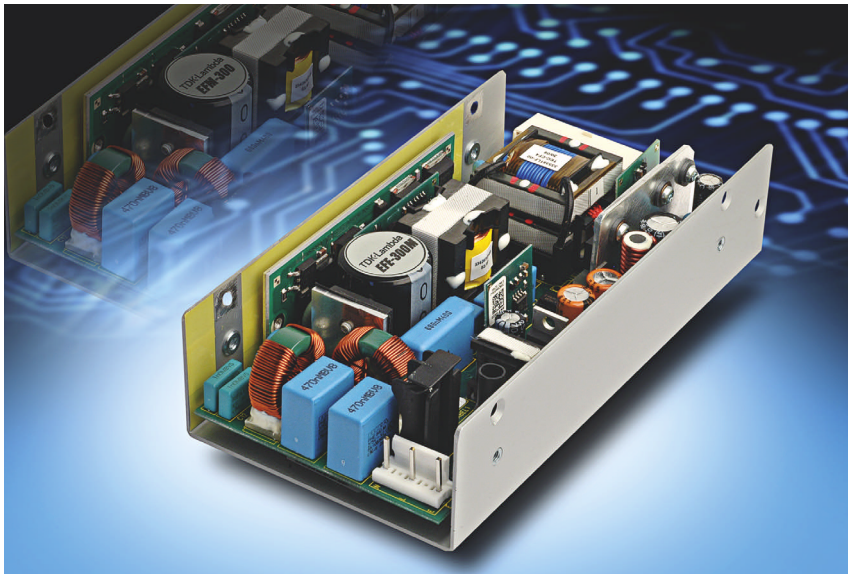


Digitally controlled power supplies meet IEC 60601-1 medical specifications

The digitally controlled EFE300M 300W power supply has 4-kV-ac reinforced input-to-output isolation and 1500V-ac output-to-ground isolation. Meeting IEC 60601-1 international-safety standards, the device suits use in B- and BF-type medical applications. The power supply delivers 300W continuous power with 400W peak for 10 seconds and has nominal outputs of 12V at 25A or 24V at 12.5A, with nonstandard output voltages available by factory programming. Measuring 3×6×1.6 in., the EFE300M series costs $183 (500).

TDK-Lambda, www.us.tdk-lambda.com

Mini-USB ac/dc-power adapters meet regional needs

The four localized models in the vendor's wall-mount DCH3 ac/dc-power-adapter series provide cableless outputs, supporting interchangeable USB-to-Mini/Micro-USB 2.0 output cables. A slim form factor makes the devices suitable for charging portable consumer-electronic devices requiring 5V-dc power supplies and using Mini-USB connectors for inputs, such as PDAs, digital cameras, and mobile phones. Features include 100 to 254V-ac inputs in the US, EU, UK, and Australian models, each configured with region-appropriate input plugs, and generation of 5V output with a 3W power capability. Meeting Energy Star Level IV efficiency standards, the DCH3 Mini-USB ac/dc-power-adapter series costs $3.99.

Emerson Network Power, www.emerson.com

Rugged dc/dc converter has 4-to-1 input ratio

The rugged VHK dc/dc-converter series features a 4-to-1 input ratio and 50 to 200W output power. Other features include a selectable input-voltage range of 9 to 36V dc or 18 to 72V dc and output voltages of 3.3, 5, 12, 15, 24, or 48V. The chassis-mount unit has a built-in heat sink, providing a −40 to +85°C operating temperature, and the 50W model operates at temperatures as high as 60°C under convection-cooled conditions. Available in a 4.25×4×4.5-in. aluminum case, the VHK series costs $125.

V-Infinity, www.v-infinity.com

PWM buck regulators aim at multiple-rail applications

Targeting multiple-rail applications, the 2-MHz MIC4742 and the 4-MHz MIC4744 dual nonsynchronous PWM (pulse-width-modulator) buck regulators have a 2A maximum load current. The ICs meet the need for a dual-regulator device for the 3.3 and 5V buses. The regulators suit wired- and wireless-broadband-communication equipment, printers, high-definition set-top boxes, and low-power FPGAs. The MIC4742 and the MIC4744 cost $2.29 and $2.70 (1000), respectively.

Micrel, www.micrel.com

Ultralow-noise dc/dc regulators suit multigigabit SERDES specifications

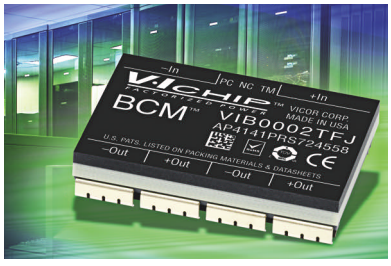
The LTM4606 and the LTM4612 dc/dc µModule regulators reduce noise by attenuating radiated energy and conducted wideband harmonic energy. Operating over a 4.5 to 28V input supply, the LTM4606 regulates 0.6 to 5V output voltages and delivers as much as 6A to the load. The LTM4606 provides high-speed multigigabit digital-data transmission in SERDES and

RocketIO applications. The devices' MOSFET gate drives have a controlled slew rate, and the units include input pi filters and shielded inductors. The LTM4612 operates over a 5 to 36V input supply, regulates 3.3 to 15V output voltage, and provides 5A to the load. The regulators have a CISPR22 Class B certification. The devices are encapsulated in a surface-mount plastic package and integrate the inductor, MOSFETs, regulator IC, and compensation network. Measuring 15×15×2.8 mm in an LGA package, the LTM4606 and the LTM4612 dc/dc µModule regulators cost $16.50 and $19.89 (1000), respectively.

Linear Technology, www.linear.com

Bus converter completes power-train conversion

The 330W 16th-brick-footprint VIB0002TFJ BCM (bus-converter module) completes the power-train conversion to processor and memory loads in high-voltage dc distribution in data centers. The device allows progression to 380V data centers, enabling conversion to the industry-recognized 48V-dc rail. Using a megahertz-switching, zero-voltage-switching, zero-current-switching sine-amplitude converter with a power density of 1150W/in.^{3}, the converter has 95% efficiency. The converter provides as much as 4000V of safety-isolated 330W power for downstream loads. The VIB0002TFJ costs $35.



Vicor Corp, www.vicorpower.com

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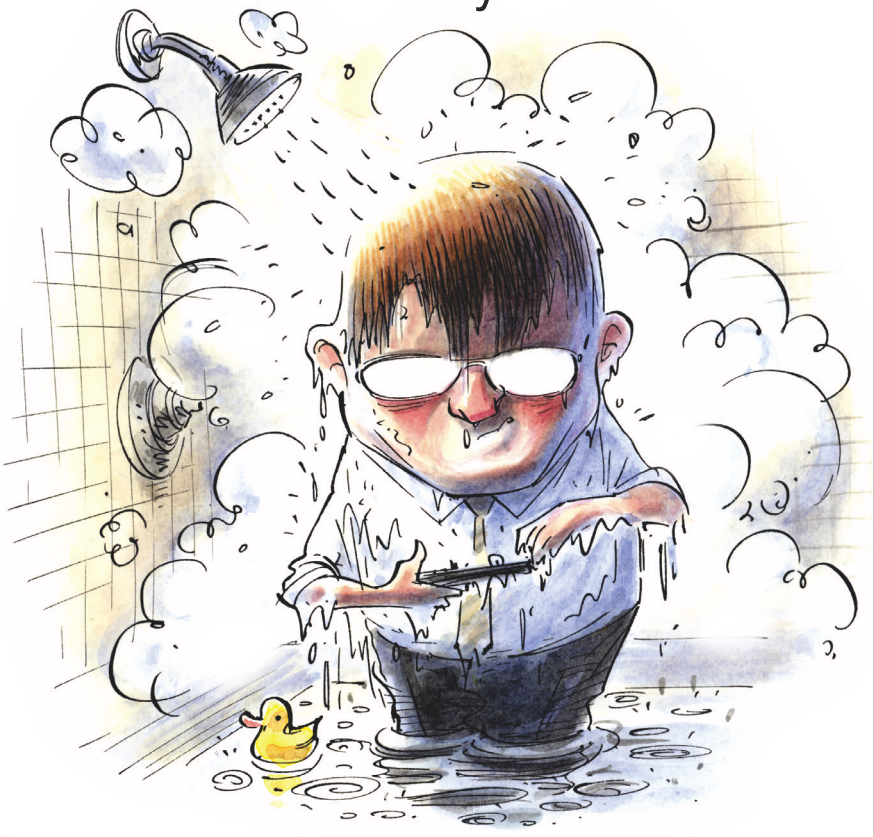
BY RICHARD RICE • INDEPENDENT CONTRACTOR

A lesson in humidity? No sweat



DANIEL VASCONCELLOS

Years ago, I started a new job as a senior engineer for a medical-device company that designed and manufactured products for use in cardiology to diagnose heart arrhythmias and other types of patient monitoring. My first assignment was to explain and fix the outrageously high failure rate of a Holter recorder. In 1961, American biophysicist Norman Holter, MD, invented the device, which uses electrodes connected to the patient's chest to record the ECG (electrocardiogram) waveform over a 24- or 48-hour period. The long recording period allows cardiologists to capture any ECG events that may occur only during certain times of the day or during certain activities, such as while a patient is sleeping or at work.

As I began to investigate, I found out that this situation had been going on for some time and customers were now demanding new units. Our repair department generally could not find anything wrong with the recorders, even though customers would send along recordings showing ECG waveforms that would "go nuts" with huge amounts of noise, swinging from rail to rail for varying periods—sometime for hours. I estimated that the company had scrapped $800,000 worth of parts.

After spending a week or two looking over schematics and talking to everyone I could find who might have a clue, I decided to do some environmental testing. Bingo. I was able to re-create the failure mechanism by raising the humidity level. As I thought about it, it all started to make sense. Patients wore the recorders to bed at night under the covers; they showered with them on. Patients entered warm rooms from the cold outdoors, causing condensation to form on the PCBs (printed-circuit boards). About two in five would fail at high humidity, and all would fail with condensation. Most would recover and work fine after they dried out, but some sustained permanent damage.

A little more investigation and a long talk with a chemist from our hybrid lab led to a conclusion: Humidity, along with hydroscopic surface contamination, absorbs moisture from the air, resulting in conductivity along the surface between traces. The leakage causes metal-migration electroplating. Branchlike structures, or dendrites, form between the traces, causing microscopic short circuits that are so small they blow open like a fuse as the current rises. The abruptly changing leakage currents were causing the noisy ECG signals. Keeping the surface clean is important but does not prevent condensation problems because the water can absorb carbon dioxide from the air, forming carbonic acid, which is conductive.

The solution was to clean, dry, and then coat the entire PCB with a conformal material to keep moisture out. It took a lot of effort to get someone to make the tough decision to go ahead with the process change. Once they got the OK, some of the engineers went to work on the weekend, and, by Monday morning, they had hooked up a dishwasher to a deionized-water source. Using that machine along with an electric oven, both from Sears, they had the conformal-coating process up and running a few days later.

So, the Holter-recorder problem had disappeared, and I was a hero for about 15 minutes. We could do nothing about the boxes of scrapped recorders or those still out in the field. EDN

Richard Rice is an independent contractor in Oconomowoc, WI, with 38 years' experience in electronics design. You can reach him at mlrice@att.net.

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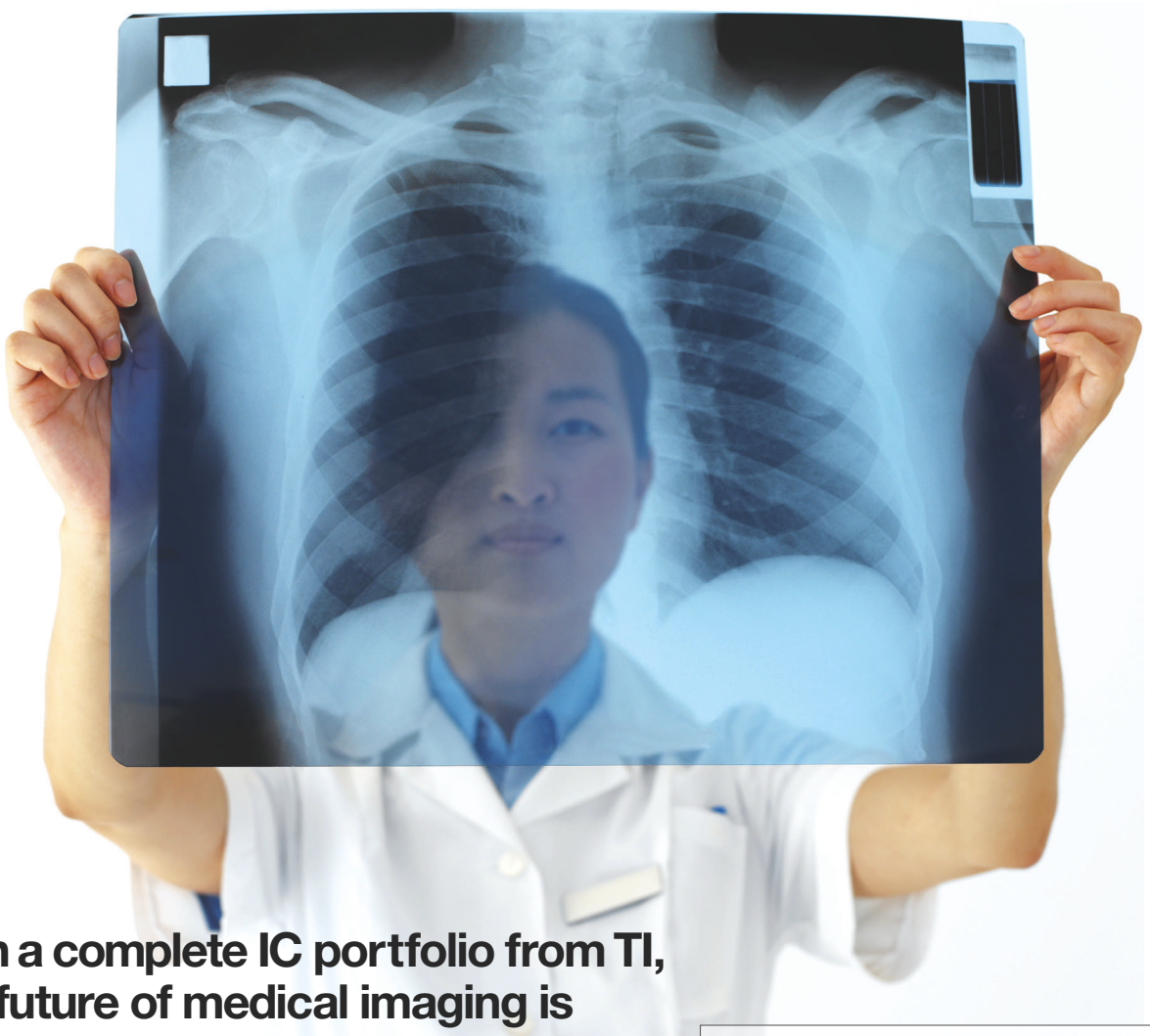

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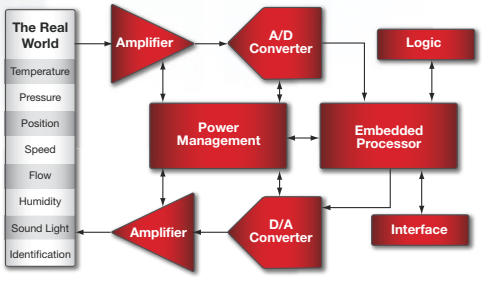

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